iPad 1 (2010) was the first popular tablet: more than 15 million sold.

iPad 1 contains 45nm Apple A4 system-on-chip.

Apple A4 contains 1GHz ARM Cortex-A8 CPU core + PowerVR SGX 535 GPU.

Cortex-A8 CPU core (2005) supports ARMv7-A insn set, including NEON vector insns. Apple A4 also appeared in iPhone 4 (2010).

45nm 1GHz Samsung Exynos 3110 in Samsung Galaxy S (2010) contains Cortex-A8 CPU core.

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More than one billion Cortex-A7 devices have been sold.

Popular in low-cost and mid-range smartphones: Mobiistar Buddy, Mobiistar Kool, Mobiistar LAI Z1, Samsung Galaxy J1 Ace Neo, etc.

Also used in typical TV boxes, Sony SmartWatch 3, Samsung Gear S2, Raspberry Pi 2, etc. signed more cores ng same ARMv7-A insns: 49 (2007),

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Basic ARM insn set uses 16 32-bit registers: 512 bits

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Cortex-A7 and Cortex-A8 (and Cortex-A15 and Cortex and Qualcomm Scorpion and Qualcomm Krait) always have NEON insns.

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NEON instruction

$$4x a = b + c$$

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Stage N2: reads b and c.

Stage N3: performs addition.

Stage N4: a is ready.

$$\mathsf{ADD} \xrightarrow{2 \mathsf{ cycles}} \mathsf{ADD} \xrightarrow{2 \mathsf{ cycles}} \mathsf{ADD}$$

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4x a = b - c

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$$a[0] = b[0] -$$

$$a[1] = b[1] -$$

$$a[2] = b[2] -$$

$$a[3] = b[3] -$$

Stage N1: reads of

Stage N2: reads b

Stage N3: perforn

Stage N4: a is rea

$$4DD \xrightarrow{2 \text{ or } 3 \text{ cycles}}$$

Also logic insns, sl

NEON instructions

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$$\mathsf{ADD} \xrightarrow{2 \mathsf{ cycles}} \mathsf{ADD} \xrightarrow{2 \mathsf{ cycles}} \mathsf{ADD}$$

4x a = b - c

is a vector of 4 32-bit subtra

$$a[0] = b[0] - c[0];$$

$$a[1] = b[1] - c[1];$$

$$a[2] = b[2] - c[2];$$

$$a[3] = b[3] - c[3].$$

Stage N1: reads c.

Stage N2: reads b, negates

Stage N3: performs addition

Stage N4: a is ready.

$$ADD \xrightarrow{2 \text{ or } 3 \text{ cycles}} SUB$$

Also logic insns, shifts, etc.

-fast,

-slow.

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4x a = b - c

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ADD $\stackrel{\text{2 or 3 cycles}}{\longrightarrow}$ SUB

Also logic insns, shifts, etc.

+ c

or of 4 32-bit additions:

$$= b[0] + c[0];$$

$$= b[1] + c[1];$$

$$= b[2] + c[2];$$

$$= b[3] + c[3].$$

A8 NEON arithmetic unit

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ADD
$$\stackrel{\text{2 or 3 cycles}}{\longrightarrow}$$
 SUB

Also logic insns, shifts, etc.

Multiplio c[0,1]

c[2,3]

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Multiply c[0,1]

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 SUB

Also logic insns, shifts, etc.

c[0,1] = a[0] sic[2,3] = a[1] s

Multiplication insr

Two cycles on Coi

Multiply-accumula c[0,1] += a[0] s

$$c[2,3] += a[1] s$$

Also two cycles or

Stage N1: reads b

Stage N2: reads a

Stage N3: reads of

Stage N8: c is rea

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es → ADD 4x a = b - c

is a vector of 4 32-bit subtractions:

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ADD
$$\stackrel{\text{2 or 3 cycles}}{\longrightarrow}$$
 SUB

Also logic insns, shifts, etc.

Multiplication insn:

$$c[0,1] = a[0] signed* b[$$

$$c[2,3] = a[1] signed* b[$$

Two cycles on Cortex-A8.

Multiply-accumulate insn:

$$c[2,3] += a[1] signed* b$$

Also two cycles on Cortex-A

Stage N1: reads b.

Stage N2: reads a.

Stage N3: reads c if accum

:

Stage N8: c is ready.

$$4x a = b - c$$

is a vector of 4 32-bit subtractions:

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Two cycles on Cortex-A8.

Multiply-accumulate insn:

Also two cycles on Cortex-A8.

Stage N1: reads b.

Stage N2: reads a.

Stage N3: reads c if accumulate.

Stage N8: c is ready.

or of 4 32-bit subtractions:

$$= b[0] - c[0];$$

$$= b[1] - c[1];$$

$$= b[2] - c[2];$$

$$= b[3] - c[3].$$

1: reads c.

3: performs addition.

4: a is ready.

ic insns, shifts, etc.

Multiplication insn:

$$c[0,1] = a[0] signed* b[0];$$

 $c[2,3] = a[1] signed* b[1]$

Two cycles on Cortex-A8.

Multiply-accumulate insn:

Also two cycles on Cortex-A8.

Stage N1: reads b.

Stage N2: reads a.

Stage N3: reads c if accumulate.

Stage N8: c is ready.

Typical:

Cortex-A

Reads c

negates c.ns addition.

- SUB

nifts, etc.

Multiplication insn:

$$c[0,1] = a[0] signed* b[0];$$

 $c[2,3] = a[1] signed* b[1]$

Two cycles on Cortex-A8.

Multiply-accumulate insn:

Also two cycles on Cortex-A8.

Stage N1: reads b.

Stage N2: reads a.

Stage N3: reads c if accumulate.

--

Stage N8: c is ready.

Typical sequence of

$$c[0,1] = a[0] si$$
 $c[2,3] = a[1] si$
 $c[0,1] += e[2] si$
 $c[2,3] += e[3] si$

$$c[0,1] += g[0] s$$

$$c[2,3] += g[1] s$$

Cortex-A8 recogni Reads c in N6 inst

$$c[0,1] = a[0] signed* b[0];$$

$$c[2,3] = a[1] signed* b[1]$$

Two cycles on Cortex-A8.

Multiply-accumulate insn:

$$c[0,1] += a[0] signed* b[0];$$

Also two cycles on Cortex-A8.

Stage N1: reads b.

Stage N2: reads a.

Stage N3: reads c if accumulate.

•

Stage N8: c is ready.

Typical sequence of three in

$$c[0,1] = a[0] signed* b[$$

 $c[2,3] = a[1] signed* b[$

$$c[2,3] += e[3] signed* f$$

$$c[0,1] += g[0] signed* h$$

$$c[2,3] += g[1] signed* h$$

Cortex-A8 recognizes this paragraph Reads c in N6 instead of N3

c[0,1] = a[0] signed* b[0];c[2,3] = a[1] signed* b[1]

Two cycles on Cortex-A8.

Multiply-accumulate insn:

c[0,1] += a[0] signed* b[0]; c[2,3] += a[1] signed* b[1]

Also two cycles on Cortex-A8.

Stage N1: reads b.

Stage N2: reads a.

Stage N3: reads c if accumulate.

•

Stage N8: c is ready.

Typical sequence of three insns:

c[0,1] = a[0] signed* b[0];
c[2,3] = a[1] signed* b[1]

c[0,1] += e[2] signed* f[2];
c[2,3] += e[3] signed* f[3]

c[0,1] += g[0] signed* h[2];
c[2,3] += g[1] signed* h[3]

Cortex-A8 recognizes this pattern. Reads c in N6 instead of N3.

cation insn:

= a[0] signed* b[0];

= a[1] signed* b[1]

les on Cortex-A8.

-accumulate insn:

+= a[0] signed* b[0];

+= a[1] signed* b[1]

cycles on Cortex-A8.

1: reads b.

2: reads a.

3: reads c if accumulate.

8: c is ready.

Typical sequence of three insns:

c[0,1] = a[0] signed* b[0];c[2,3] = a[1] signed* b[1]

c[0,1] += e[2] signed* f[2];c[2,3] += e[3] signed* f[3]

c[0,1] += g[0] signed* h[2];

c[2,3] += g[1] signed* h[3]

Cortex-A8 recognizes this pattern.

Reads c in N6 instead of N3.

```
Time N1
    5 h
    6
   10
   11
```

if accumulate.

ıdy.

Typical sequence of three insns:

$$c[0,1] += g[0] signed* h[2];$$

$$c[2,3] += g[1] signed* h[3]$$

Cortex-A8 recognizes this pattern.

Reads c in N6 instead of N3.

N1	N2	N 3	N
b			
	a		
f		×	
	e		×
h		×	
	g		×
		X	
			×
	b f	b a f e h	$egin{array}{c c} a & \times & \times \\ e & \times & \end{array}$

[0];

[0];

ulate.

[1]

Typical sequence of three insns:

$$c[0,1] = a[0] signed* b[0];$$

 $c[2,3] = a[1] signed* b[1]$

$$c[2,3] += e[3] signed* f[3]$$

$$c[0,1] += g[0] signed* h[2];$$

$$c[2,3] += g[1] signed* h[3]$$

Cortex-A8 recognizes this pattern.

Reads c in N6 instead of N3.

Time	N1	N2	N3	N4	N5	N6	N7	N8
1	b							
2		a						
2 3	f		X					
4		e		×				
5	h		×		×			
6		g		X		×		
7			×		X			
8				X		×		C
9					X		+	
10						X		C
11							+	
12								C

sequence of three insns:

A8 recognizes this pattern.

in N6 instead of N3.

Time	N1	N2	N 3	N4	N5	N6	N7	N8
1	b							
2		a						
2 3	f		×					
4		e		×				
5	h		×		×			
6		g		X		X		
7			X		X			
8				X		X		C
9					×		+	
10						×		C
11							+	
12								C

NEON a and perr r = s[1]

Cortex-ANEON In that run

NEON a

Arithme most im can ofte to hide I

Cortex-*A* handling

of three insns:

igned* b[0];

igned* b[1]

signed* f[2];

signed* f[3]

signed* h[2];

signed* h[3]

zes this pattern.

tead of N3.

Time	N1	N2	N 3	N4	N5	N6	N7	N8
1	b							
2		а						
3	f		×					
4		e		×				
5	h		×		×			
6		g		X		X		
7			X		X			
8				X		X		C
9					X		+	
10						X		C
11							+	
12								C

NEON also has loand permutation in results and results and results are selected as a selected as loand permutation in the results are selected as loand permutation are selected as loand permutation and results are selected as loand permutation are selected as loand permutation and results are selected as loand permutation are selected as loan

Cortex-A8 has a set NEON load/store that runs in parallel NEON arithmetic

Arithmetic is typic most important be can often schedule to hide loads/store

Cortex-A7 is differ handling all NEON

10

sns:

[0];

1]

[2];

[2];

attern.

[3]

[3]

NEON also has load/store in and permutation insns: e.g., r = s[1] t[2] r[2,3]

Cortex-A8 has a separate NEON load/store unit that runs in parallel with NEON arithmetic unit.

Arithmetic is typically most important bottleneck: can often schedule insns to hide loads/stores/perms.

Cortex-A7 is different: one in handling all NEON insus.

Time	N1	N2	N3	N4	N5	N6	N7	N8
1	b							
2 3		a						
3	f		X					
4		e		X				
5	h		X		X			
6		g		X		X		
7			×		×			
8				X		X		C
9					X		+	
10						X		C
11							+	
12								C

NEON also has load/store insns and permutation insns: e.g., r = s[1] t[2] r[2,3]

Cortex-A8 has a separate NEON load/store unit that runs in parallel with NEON arithmetic unit.

11

Arithmetic is typically most important bottleneck: can often schedule insns to hide loads/stores/perms.

Cortex-A7 is different: one unit handling all NEON insns.

-	N2	N 3	N4	N5	N6	N7	N8
	a						
		X					
	e		×				
		X		X			
	g		X		×		
		X		X			
			×		X		C
				×		+	
					×		C
						+	
							C

NEON also has load/store insns and permutation insns: e.g., r = s[1] t[2] r[2,3]

Cortex-A8 has a separate NEON load/store unit that runs in parallel with NEON arithmetic unit.

11

Arithmetic is typically most important bottleneck: can often schedule insns to hide loads/stores/perms.

Cortex-A7 is different: one unit handling all NEON insns.

Curve25 Radix 2² (f_0, f_1, f_2) to repres $f = f_0 2^{102}f_4 +$ $2^{204}f_8 +$ Unscaled f is valu $f_0 t^0 + 2$

 f_4t^4+2

 $f_8t^8 + 2$

NEON also has load/store insns and permutation insns: e.g., r = s[1] t[2] r[2,3]

Cortex-A8 has a separate NEON load/store unit that runs in parallel with NEON arithmetic unit.

Arithmetic is typically most important bottleneck: can often schedule insns to hide loads/stores/perms.

Cortex-A7 is different: one unit handling all NEON insns.

Curve25519 on NE

Radix $2^{25.5}$: Use s $(f_0, f_1, f_2, f_3, f_4, f_5, f_5)$ to represent the in $f = f_0 + 2^{26}f_1 + 2^{25}f_5 + 2^{2504}f_8 + 2^{2504}f_8 + 2^{2504}f_9$ mo

Unscaled polynom f is value at $2^{25.5}$ $f_0t^0 + 2^{0.5}f_1t^1 + t^4$ $f_4t^4 + 2^{0.5}f_5t^5 + t^6$ $f_8t^8 + 2^{0.5}f_0t^9$.

11

NEON also has load/store insns and permutation insns: e.g.,

r = s[1] t[2] r[2,3]

Cortex-A8 has a separate NEON load/store unit that runs in parallel with NEON arithmetic unit.

Arithmetic is typically most important bottleneck: can often schedule insns to hide loads/stores/perms.

Cortex-A7 is different: one unit handling all NEON insns.

Curve25519 on NEON

Radix 2^{25.5}: Use small integ $(f_0, f_1, f_2, f_3, f_4, f_5, f_6, f_7, f_8, f_9)$ to represent the integer $f = f_0 + 2^{26}f_1 + 2^{51}f_2 + 2^7$ $2^{102}f_4 + 2^{128}f_5 + 2^{153}f_6 + 2^{1}$ $2^{204}f_8 + 2^{230}f_9$ modulo 2^{255}

Unscaled polynomial view: f is value at $2^{25.5}$ of the po $f_0 t^0 + 2^{0.5} f_1 t^1 + f_2 t^2 + 2^{0.5}$ $f_4t^4 + 2^{0.5}f_5t^5 + f_6t^6 + 2^{0.5}$ $f_8t^8 + 2^{0.5}f_0t^9$.

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NEON also has load/store insns and permutation insns: e.g., r = s[1] t[2] r[2,3]

Cortex-A8 has a separate NEON load/store unit that runs in parallel with NEON arithmetic unit.

Arithmetic is typically most important bottleneck: can often schedule insns to hide loads/stores/perms.

Cortex-A7 is different: one unit handling all NEON insns.

Curve25519 on NEON

Radix $2^{25.5}$: Use small integers $(f_0, f_1, f_2, f_3, f_4, f_5, f_6, f_7, f_8, f_9)$ to represent the integer $f = f_0 + 2^{26}f_1 + 2^{51}f_2 + 2^{77}f_3 + 2^{102}f_4 + 2^{128}f_5 + 2^{153}f_6 + 2^{179}f_7 + 2^{204}f_8 + 2^{230}f_9$ modulo $2^{255} - 19$.

Unscaled polynomial view: f is value at $2^{25.5}$ of the poly $f_0t^0 + 2^{0.5}f_1t^1 + f_2t^2 + 2^{0.5}f_3t^3 + f_4t^4 + 2^{0.5}f_5t^5 + f_6t^6 + 2^{0.5}f_7t^7 + f_8t^8 + 2^{0.5}f_0t^9$.

Iso has load/store insns nutation insns: e.g.,

] t[2] r[2,3]

A8 has a separate oad/store unit s in parallel with rithmetic unit.

tic is typically portant bottleneck: n schedule insns oads/stores/perms.

A7 is different: one unit all NEON insns.

Curve25519 on NEON

Radix 2^{25.5}: Use small integers $(f_0, f_1, f_2, f_3, f_4, f_5, f_6, f_7, f_8, f_9)$ to represent the integer $f = f_0 + 2^{26}f_1 + 2^{51}f_2 + 2^{77}f_3 + 2^{11}f_2 + 2^{11}f_3 + 2^{11}$ $2^{102}f_4 + 2^{128}f_5 + 2^{153}f_6 + 2^{179}f_7 +$ $2^{204}f_8 + 2^{230}f_9$ modulo $2^{255} - 19$.

Unscaled polynomial view:

f is value at $2^{25.5}$ of the poly $f_0t^0 + 2^{0.5}f_1t^1 + f_2t^2 + 2^{0.5}f_3t^3 +$ $f_4t^4 + 2^{0.5}f_5t^5 + f_6t^6 + 2^{0.5}f_7t^7 +$ $f_8 t^8 + 2^{0.5} f_0 t^9$.

$$h \equiv fg$$

$$h_0 = f_0 g_0$$
 $h_1 = f_0 g_1$
 $h_2 = f_0 g_2$

$$h_3 = f_0 g_3$$

 $h_4 = f_0 g_4$

$$h_5=f_0g_5$$

$$h_6=f_0g_6$$

$$h_7 = f_0 g_7$$

$$h_8 = f_0 g_8$$

$$h_9 = f_0 g_9$$

Proof: r

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unit
el with
unit.

[2,3]

cally ottleneck: e insns es/perms.

ent: one unit linsns.

Curve25519 on NEON

Radix $2^{25.5}$: Use small integers $(f_0, f_1, f_2, f_3, f_4, f_5, f_6, f_7, f_8, f_9)$ to represent the integer $f = f_0 + 2^{26}f_1 + 2^{51}f_2 + 2^{77}f_3 + 2^{102}f_4 + 2^{128}f_5 + 2^{153}f_6 + 2^{179}f_7 + 2^{204}f_8 + 2^{230}f_9$ modulo $2^{255} - 19$.

Unscaled polynomial view:

f is value at $2^{25.5}$ of the poly $f_0t^0 + 2^{0.5}f_1t^1 + f_2t^2 + 2^{0.5}f_3t^3 + f_4t^4 + 2^{0.5}f_5t^5 + f_6t^6 + 2^{0.5}f_7t^7 + f_8t^8 + 2^{0.5}f_9t^9$.

$$h \equiv fg \pmod{2^{25}}$$
 $h_0 = f_0g_0 + 38f_1g_9 + 19f_1g_0 + 19f_2g_1 + f_1g_0 + 19f_2g_2 + 2f_1g_1 + f_1g_2 + f_1g_2 + f_1g_3 + f_1g_2 + f_1g_3 + f_1g_4 + f_1g_2 + f_1g_3 + f_1g_4 + f_1g_1g_3 + f_1g_2 + f_1g_1g_3 + f_1g_1g_1 + f_1g_1g_2 + f_1g_1g_1 + f_1g_1g_2 + f_1g_1g_1 + f_1g_1g_1 + f_1g_1g_1 + f_1g_1g_2 + f_1g_1g_1 + f_1g_1g_1$

Proof: multiply po

nsns

Curve25519 on NEON

Radix $2^{25.5}$: Use small integers $(f_0, f_1, f_2, f_3, f_4, f_5, f_6, f_7, f_8, f_9)$ to represent the integer $f = f_0 + 2^{26}f_1 + 2^{51}f_2 + 2^{77}f_3 + 2^{102}f_4 + 2^{128}f_5 + 2^{153}f_6 + 2^{179}f_7 + 2^{204}f_8 + 2^{230}f_9$ modulo $2^{255} - 19$.

Unscaled polynomial view:

f is value at $2^{25.5}$ of the poly $f_0t^0 + 2^{0.5}f_1t^1 + f_2t^2 + 2^{0.5}f_3t^3 + f_4t^4 + 2^{0.5}f_5t^5 + f_6t^6 + 2^{0.5}f_7t^7 + f_8t^8 + 2^{0.5}f_9t^9$.

unit

 $h \equiv fg \pmod{2^{255} - 19}$ w $h_0 = f_0 g_0 + 38 f_1 g_9 + 19 f_2 g_8 + 38 f_3 g_9$ $h_1 = f_0 g_1 + f_1 g_0 + 19 f_2 g_9 + 19 f_3 g_1$ $h_2 = f_0 g_2 + 2f_1 g_1 + f_2 g_0 + 38f_3 g_1$ $h_3 = f_0 g_3 + f_1 g_2 + f_2 g_1 + f_3 g_1$ $h_4 = f_0 g_4 + 2f_1 g_3 + f_2 g_2 + 2f_3 g_4$ $h_5 = f_0 g_5 + f_1 g_4 + f_2 g_3 + f_3 g_4$ $h_6 = f_0 g_6 + 2f_1 g_5 + f_2 g_4 + 2f_3 g_6$ $h_7 = f_0 g_7 + f_1 g_6 + f_2 g_5 + f_3 g_6$ $h_8 = f_0 g_8 + 2f_1 g_7 + f_2 g_6 + 2f_3 g_8$ $h_9 = f_0 g_9 + f_1 g_8 + f_2 g_7 + f_3 g_8$

Proof: multiply polys mod t

Curve25519 on NEON

Radix $2^{25.5}$: Use small integers $(f_0, f_1, f_2, f_3, f_4, f_5, f_6, f_7, f_8, f_9)$ to represent the integer $f = f_0 + 2^{26}f_1 + 2^{51}f_2 + 2^{77}f_3 + 2^{102}f_4 + 2^{128}f_5 + 2^{153}f_6 + 2^{179}f_7 + 2^{204}f_8 + 2^{230}f_9$ modulo $2^{255} - 19$.

Unscaled polynomial view:

f is value at $2^{25.5}$ of the poly $f_0t^0 + 2^{0.5}f_1t^1 + f_2t^2 + 2^{0.5}f_3t^3 + f_4t^4 + 2^{0.5}f_5t^5 + f_6t^6 + 2^{0.5}f_7t^7 + f_8t^8 + 2^{0.5}f_9t^9$.

 $h \equiv fg \pmod{2^{255} - 19}$ where

$$h_0 = f_0 g_0 + 38 f_1 g_9 + 19 f_2 g_8 + 38 f_3 g_7 + 19 f_4 g_6 + h_1 = f_0 g_1 + f_1 g_0 + 19 f_2 g_9 + 19 f_3 g_8 + 19 f_4 g_7 + h_2 = f_0 g_2 + 2 f_1 g_1 + f_2 g_0 + 38 f_3 g_9 + 19 f_4 g_8 + h_3 = f_0 g_3 + f_1 g_2 + f_2 g_1 + f_3 g_0 + 19 f_4 g_9 + h_4 = f_0 g_4 + 2 f_1 g_3 + f_2 g_2 + 2 f_3 g_1 + f_4 g_0 + h_5 = f_0 g_5 + f_1 g_4 + f_2 g_3 + f_3 g_2 + f_4 g_1 + h_6 = f_0 g_6 + 2 f_1 g_5 + f_2 g_4 + 2 f_3 g_3 + f_4 g_2 + h_7 = f_0 g_7 + f_1 g_6 + f_2 g_5 + f_3 g_4 + f_4 g_3 + h_8 = f_0 g_8 + 2 f_1 g_7 + f_2 g_6 + 2 f_3 g_5 + f_4 g_4 + h_9 = f_0 g_9 + f_1 g_8 + f_2 g_7 + f_3 g_6 + f_4 g_5 + f_4 g_5 + f_4 g_6 + f_4 g_5 + f_4 g_6 +$$

Proof: multiply polys mod $t^{10} - 19$.

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^{25.5}: Use small integers

$$f_{3}, f_{4}, f_{5}, f_{6}, f_{7}, f_{8}, f_{9}$$

sent the integer

$$-2^{26}f_1 + 2^{51}f_2 + 2^{77}f_3 + 2^{128}f_5 + 2^{153}f_6 + 2^{179}f_7 + 2^{128}f_5 + 2^{153}f_6 + 2^{179}f_7 + 2^{17$$

 $2^{230} f_9$ modulo $2^{255} - 19$.

d polynomial view:

e at $2^{25.5}$ of the poly

$$^{0.5}f_1t^1 + f_2t^2 + 2^{0.5}f_3t^3 +$$

$$^{0.5}f_5t^5 + f_6t^6 + 2^{0.5}f_7t^7 +$$

 $0.5 f_9 t^9$.

$$h \equiv fg \pmod{2^{255} - 19}$$
 where

$$h_0 = f_0 g_0 + 38 f_1 g_9 + 19 f_2 g_8 + 38 f_3 g_7 + 19 f_4 g_6 + 38 f_5 g_5 + 19 f_4 g_6 + f_1 g_0 + 19 f_2 g_9 + 19 f_3 g_8 + 19 f_4 g_7 + 19 f_5 g_6 + 19 f_4 g_8 + 19 f_4 g_8 + 19 f_5 g_6 + 19 f_4 g_8 + 19 f_5 g_8 + 19 f_4 g_9 + 19 f_5 g_8 + 19 f_8 g_9 + 19$$

Proof: multiply polys mod $t^{10} - 19$.

 $f_5g_4+ f_6g_3+ f_7g_2$

<u>EON</u>

small integers

$$f_6$$
, f_7 , f_8 , f_9)

teger

$$2^{51}f_2 + 2^{77}f_3 +$$

$$2^{153}f_6 + 2^{179}f_7 +$$

odulo $2^{255} - 19$.

ial view:

of the poly

$$f_2t^2 + 2^{0.5}f_3t^3 +$$

$$f_6t^6 + 2^{0.5}f_7t^7 +$$

 $h \equiv fg \pmod{2^{255} - 19}$ where

Proof: multiply polys mod $t^{10} - 19$.

 $h_9 = f_0 g_9 + f_1 g_8 + f_2 g_7 + f_3 g_6 + f_4 g_5 +$

ers

 $^{7}f_{3} +$

 $^{.79}f_7 +$

-19.

 $f_3t^3 +$

 $f_7 t^7 +$

 $h \equiv fg \pmod{2^{255} - 19}$ where

 $h_0 = f_0 g_0 + 38 f_1 g_9 + 19 f_2 g_8 + 38 f_3 g_7 + 19 f_4 g_6 + 38 f_5 g_5 + 19 f_6 g_4 + 38 f_7 g_3 + 19 f_8 g_2 + 38 f_8 g_8 +$ $h_2 = f_0 g_2 + 2f_1 g_1 +$ $h_3 = f_0 g_3 +$ $f_1g_2 +$ $f_2g_1 +$ $h_4 = f_0 g_4 + 2f_1 g_3 +$ $f_2g_2 + 2f_3g_1 +$ $f_1g_4 +$ $h_5 = f_0 g_5 +$ $f_2g_3 + f_3g_2 +$ $f_4g_1 +$ $h_6 = f_0 g_6 + 2f_1 g_5 +$ $f_2g_4 + 2f_3g_3 +$ $h_7 = f_0 g_7 + f_1 g_6 +$ $f_3g_4 +$ $f_4g_3 +$ $f_2g_5 +$ $h_8 = f_0 g_8 + 2f_1 g_7 +$ $f_2g_6 + 2f_3g_5 +$ $f_4g_4 +$ $f_2g_7 +$ $f_3g_6 +$ $f_4g_5 +$ $h_9 = f_0 g_9 + f_1 g_8 +$

Proof: multiply polys mod $t^{10} - 19$.

 $f_1g_0 + 19f_2g_9 + 19f_3g_8 + 19f_4g_7 + 19f_5g_6 + 19f_6g_5 + 19f_7g_4 + 19f_8g_3 + 1$ $f_2g_0 + 38f_3g_9 + 19f_4g_8 + 38f_5g_7 + 19f_6g_6 + 38f_7g_5 + 19f_8g_4 + 3$ $f_3g_0 + 19f_4g_9 + |19f_5g_8 + 19f_6g_7 + 19f_7g_6 + 19f_8g_5 + 1$ $f_4g_0 + 38f_5g_9 + 19f_6g_8 + 38f_7g_7 + 19f_8g_6 + 3$ $f_5g_0+19f_6g_9+19f_7g_8+19f_8g_7+1$ $f_4g_2 + 2f_5g_1 + f_6g_0 + 38f_7g_9 + 19f_8g_8 + 3$ $f_5g_2+ f_6g_1+ f_7g_0+19f_8g_9+1$ $2f_5g_3 + f_6g_2 + 2f_7g_1 +$ $f_8g_0 + 3$ f_5g_4+ $f_6g_3 + f_7g_2 + f_8g_1 +$

 $h \equiv fg \pmod{2^{255} - 19}$ where

Proof: multiply polys mod $t^{10} - 19$.

$$(\text{mod } 2^{255} - 19) \text{ where}$$

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$$+ f_1 g_0 + 19 f_2 g_3 + 30 f_3 g_7 + 19 f_4 g_6 + f_1 g_0 + 19 f_2 g_9 + 19 f_3 g_8 + 19 f_4 g_7 + f_2 g_0 + 38 f_3 g_9 + 19 f_4 g_8 + f_1 g_2 + f_2 g_1 + f_3 g_0 + 19 f_4 g_9 + f_2 g_1 + f_2 g_2 + 2 f_3 g_1 + f_4 g_0 + f_1 g_4 + f_2 g_3 + f_3 g_2 + f_4 g_1 + f_2 g_4 + 2 f_3 g_3 + f_4 g_2 + f_2 g_4 + 2 f_3 g_3 + f_4 g_2 + f_1 g_6 + f_2 g_5 + f_3 g_4 + f_4 g_3 + f_4 g_3 + f_4 g_4 + f_1 g_8 + f_2 g_7 + f_3 g_6 + f_4 g_5 + f_4 g_6 + f_4 g_5 + f_4 g_6 +$$

nultiply polys mod $t^{10} - 19$.

 $+38f_{1}g_{9}+19f_{2}g_{8}+38f_{3}g_{7}+19f_{4}g_{6}+38f_{5}g_{5}+19f_{6}g_{4}+38f_{7}g_{3}+19f_{8}g_{2}+38f_{9}g_{1}$ $+ f_1g_0 + 19f_2g_9 + 19f_3g_8 + 19f_4g_7 + 19f_5g_6 + 19f_6g_5 + 19f_7g_4 + 19f_8g_3 + 19f_9g_2$ $f_2g_0 + 38f_3g_9 + 19f_4g_8 + 38f_5g_7 + 19f_6g_6 + 38f_7g_5 + 19f_8g_4 + 38f_9g_3$ $f_2g_1 + f_3g_0 + 19f_4g_9 + 19f_5g_8 + 19f_6g_7 + 19f_7g_6 + 19f_8g_5 + 19f_9g_4$ $f_4g_0 + 38f_5g_9 + 19f_6g_8 + 38f_7g_7 + 19f_8g_6 + 38f_9g_5$ $f_5g_0+19f_6g_9+19f_7g_8+19f_8g_7+19f_9g_6$, $2f_5g_1 + f_6g_0 + 38f_7g_9 + 19f_8g_8 + 38f_9g_7$ $f_5g_2 +$ $f_6g_1 + f_7g_0 + 19f_8g_9 + 19f_9g_8$ $f_8g_0+38f_9g_9$, $2f_5g_3+$ $f_6g_2 + 2f_7g_1 +$ $f_5g_4 +$ $f_6g_3 + f_7g_2 +$ $f_8g_1 +$ f_0g_0 .

Each h_i products of $2f_1$, 2 $19g_1, 19$

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 $h_0, h_1, ...$

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 $f_2g_5 +$ $f_2g_7 + f_3g_6 +$ olys mod $t^{10} - 19$.

 $9f_2g_8 + 38f_3g_7 + 19f_4g_6 + 38f_5g_5 + 19f_6g_4 + 38f_7g_3 + 19f_8g_2 + 38f_9g_1$ $9f_2g_9 + 19f_3g_8 + 19f_4g_7 + 19f_5g_6 + 19f_6g_5 + 19f_7g_4 + 19f_8g_3 + 19f_9g_2$ $f_2g_0 + 38f_3g_9 + 19f_4g_8 + 38f_5g_7 + 19f_6g_6 + 38f_7g_5 + 19f_8g_4 + 38f_9g_3$ $f_2g_1 + f_3g_0 + 19f_4g_9 + 19f_5g_8 + 19f_6g_7 + 19f_7g_6 + 19f_8g_5 + 19f_9g_4$ $f_2g_2 + 2f_3g_1 + f_4g_0 + 38f_5g_9 + 19f_6g_8 + 38f_7g_7 + 19f_8g_6 + 38f_9g_5$ f_2g_3+ f_3g_2+ f_4g_1+ $f_5g_0+19f_6g_9+19f_7g_8+19f_8g_7+19f_9g_6$, $f_2g_4 + 2f_3g_3 + f_4g_2 + 2f_5g_1 + f_6g_0 + 38f_7g_9 + 19f_8g_8 + 38f_9g_7$ $f_3g_4+ f_4g_3+ f_5g_2+ f_6g_1+ f_7g_0+19f_8g_9+19f_9g_8,$ $f_2g_6 + 2f_3g_5 + f_4g_4 + 2f_5g_3 + f_6g_2 + 2f_7g_1 + f_8g_0 + 38f_9g_9$ $f_4g_5+ f_5g_4+ f_6g_3+ f_7g_2+ f_8g_1+ f_9g_0.$

Each h_i is a sum of products after pred of $2f_1$, $2f_3$, $2f_5$, $2f_7$ $19g_1, 19g_2, \ldots, 19$ Each *h_i* fits into 6 under reasonable l sizes of f_1, g_1, \ldots

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 h_0, h_1, \ldots are too for subsequent mu

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 $s_1 + 1$ $r_2 +$ $r_3 +$ 54 + 15+

 $e^{10} - 19$.

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 $g_7 + 19f_4g_6 + 38f_5g_5 + 19f_6g_4 + 38f_7g_3 + 19f_8g_2 + 38f_9g_1$, $g_8 + 19f_4g_7 + |19f_5g_6 + 19f_6g_5 + 19f_7g_4 + 19f_8g_3 + 19f_9g_2$ $g_9 + 19f_4g_8 + 38f_5g_7 + 19f_6g_6 + 38f_7g_5 + 19f_8g_4 + 38f_9g_3$ $g_0 + 19f_4g_9 + 19f_5g_8 + 19f_6g_7 + 19f_7g_6 + 19f_8g_5 + 19f_9g_4$ $f_4g_0 + 38f_5g_9 + 19f_6g_8 + 38f_7g_7 + 19f_8g_6 + 38f_9g_5$ $f_4g_1+f_5g_0+19f_6g_9+19f_7g_8+19f_8g_7+19f_9g_6$ $f_4g_2 + 2f_5g_1 + f_6g_0 + 38f_7g_9 + 19f_8g_8 + 38f_9g_7$ $f_4g_3+f_5g_2+f_6g_1+f_7g_0+19f_8g_9+19f_9g_8$ $f_4g_4+2f_5g_3+f_6g_2+2f_7g_1+f_8g_0+38f_9g_9$ $f_4g_5+ | f_5g_4+ | f_6g_3+ | f_7g_2+ | f_8g_1+ | f_9g_0.$

Each h_i is a sum of ten products after precomputati of $2f_1$, $2f_3$, $2f_5$, $2f_7$, $2f_9$, $19g_1, 19g_2, \ldots, 19g_9$.

Each h_i fits into 64 bits under reasonable limits on sizes of $f_1, g_1, ..., f_9, g_9$.

(Analyze this very carefully: bugs can slip past most test See 2011 Brumley-Page-Barbosa–Vercauteren and several recent OpenSSL bug

 h_0, h_1, \ldots are too large for subsequent multiplication

$$38f_5g_5 + 19f_6g_4 + 38f_7g_3 + 19f_8g_2 + 38f_9g_1,$$
 $19f_5g_6 + 19f_6g_5 + 19f_7g_4 + 19f_8g_3 + 19f_9g_2,$
 $38f_5g_7 + 19f_6g_6 + 38f_7g_5 + 19f_8g_4 + 38f_9g_3,$
 $19f_5g_8 + 19f_6g_7 + 19f_7g_6 + 19f_8g_5 + 19f_9g_4,$
 $38f_5g_9 + 19f_6g_8 + 38f_7g_7 + 19f_8g_6 + 38f_9g_5,$
 $f_5g_0 + 19f_6g_9 + 19f_7g_8 + 19f_8g_7 + 19f_9g_6,$
 $2f_5g_1 + f_6g_0 + 38f_7g_9 + 19f_8g_8 + 38f_9g_7,$
 $f_5g_2 + f_6g_1 + f_7g_0 + 19f_8g_9 + 19f_9g_8,$
 $2f_5g_3 + f_6g_2 + 2f_7g_1 + f_8g_0 + 38f_9g_9,$
 $f_5g_4 + f_6g_3 + f_7g_2 + f_8g_1 + f_9g_0.$

Each h_i is a sum of ten products after precomputation of $2f_1, 2f_3, 2f_5, 2f_7, 2f_9, 19g_1, 19g_2, \dots, 19g_9.$

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 h_0, h_1, \dots are too large for subsequent multiplication.

 $f_6g_4 + 38f_7g_3 + 19f_8g_2 + 38f_9g_1$ $f_6g_5+19f_7g_4+19f_8g_3+19f_9g_2$ $f_6g_6 + 38f_7g_5 + 19f_8g_4 + 38f_9g_3$ $f_{6}g_{7}+19f_{7}g_{6}+19f_{8}g_{5}+19f_{9}g_{4}$ $f_6g_8 + 38f_7g_7 + 19f_8g_6 + 38f_9g_5$ $f_6g_9 + 19f_7g_8 + 19f_8g_7 + 19f_9g_6$ $f_6g_0 + 38f_7g_9 + 19f_8g_8 + 38f_9g_7$ $f_6g_1 + f_7g_0 + 19f_8g_9 + 19f_9g_8$ $f_6g_2 + 2f_7g_1 + f_8g_0 + 38f_9g_9$

 $f_6g_3 + f_7g_2 + f_8g_1 + f_9g_0$

Each h_i is a sum of ten products after precomputation of $2f_1, 2f_3, 2f_5, 2f_7, 2f_9, 19g_1, 19g_2, \dots, 19g_9.$

Each h_i fits into 64 bits under reasonable limits on sizes of $f_1, g_1, \ldots, f_9, g_9$.

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 h_0, h_1, \dots are too large for subsequent multiplication.

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- Mix si
- Interle

 $+19f_8g_2+38f_9g_1$, $+19f_8g_3+19f_9g_2$, $+19f_8g_4+38f_9g_3$, $+19f_8g_5+19f_9g_4$ $+19f_8g_6+38f_9g_5$, $+19f_8g_7+19f_9g_6$, $+19f_8g_8+38f_9g_7$ $+19f_8g_9+19f_9g_8$, $+ f_8g_0 + 38f_9g_9$, $+ f_8g_1 + f_9g_0$. Each h_i is a sum of ten products after precomputation of $2f_1, 2f_3, 2f_5, 2f_7, 2f_9, 19g_1, 19g_2, ..., 19g_9.$

Each h_i fits into 64 bits under reasonable limits on sizes of $f_1, g_1, \ldots, f_9, g_9$.

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 h_0, h_1, \dots are too large for subsequent multiplication.

Carry $h_0 \rightarrow h_1$: i.e replace (h_0, h_1) with $(h_0 \mod 2^{26}, h_1 + 1)$ This makes h_0 sm

Similarly for other Eventually all h_i a

We actually use si Slightly more expe (given details of in but more room for

Some things we ha

- Mix signed, unsi
- Interleave reduc

 $8f_9g_1$, $9f_9g_2$, 8*f*9*g*3, $9f_9g_4$, 8*f*9*g*5, 9f₉g₆, 8*f*9*g*7, $9f_9g_8$, 8*f*9*g*9, f_0g_0 .

Each h_i is a sum of ten products after precomputation of $2f_1$, $2f_3$, $2f_5$, $2f_7$, $2f_9$, $19g_1$, $19g_2$, . . . , $19g_9$.

Each h_i fits into 64 bits under reasonable limits on sizes of $f_1, g_1, \ldots, f_9, g_9$.

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 h_0, h_1, \dots are too large for subsequent multiplication.

Carry $h_0 \rightarrow h_1$: i.e., replace (h_0, h_1) with $(h_0 \mod 2^{26}, h_1 + \lfloor h_0/2^{26} \rfloor)$ This makes h_0 small.

Similarly for other h_i . Eventually all h_i are small e

We actually use signed coeff Slightly more expensive carr (given details of insn set) but more room for $ab + c^2$

Some things we haven't trie

- Mix signed, unsigned carri
- Interleave reduction, carry

Each h_i is a sum of ten products after precomputation of $2f_1, 2f_3, 2f_5, 2f_7, 2f_9, 19g_1, 19g_2, ..., 19g_9.$

Each h_i fits into 64 bits under reasonable limits on sizes of $f_1, g_1, \ldots, f_9, g_9$.

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Similarly for other h_i . Eventually all h_i are small enough.

We actually use signed coeffs. Slightly more expensive carries (given details of insn set) but more room for $ab + c^2$ etc.

Some things we haven't tried yet:

- Mix signed, unsigned carries.
- Interleave reduction, carrying.

is a sum of ten after precomputation f_3 , $2f_5$, $2f_7$, $2f_9$, g_2 , . . . , $19g_9$.

fits into 64 bits asonable limits on $f_1, g_1, \ldots, f_9, g_9$.

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are too large equent multiplication.

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Example $h_2 \rightarrow h_3$ $h_7 \rightarrow h_8$

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large Itiplication. Carry $h_0 \rightarrow h_1$: i.e., replace (h_0, h_1) with $(h_0 \mod 2^{26}, h_1 + \lfloor h_0/2^{26} \rfloor)$. This makes h_0 small.

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Minor challenge: partial Result of each instruction used until a few cylindrical challenge: partial results of each instruction of the cylindrical results of each instruction of the cylindrical results of the c

Find an independent for the CPU to standard while the first instance.

Sometimes helps thigher-level compu

Example: carries $h_1 \rightarrow h_2 \rightarrow h_3 \rightarrow h_4 \rightarrow h_7 \rightarrow h_8 \rightarrow h_9 \rightarrow h_9 \rightarrow h_1 \rightarrow h_1 \rightarrow h_2 \rightarrow h_1 \rightarrow h_2 \rightarrow h_2 \rightarrow h_3 \rightarrow h_3 \rightarrow h_1 \rightarrow h_2 \rightarrow h_2 \rightarrow h_3 \rightarrow h_3 \rightarrow h_3 \rightarrow h_3 \rightarrow h_3 \rightarrow h_3 \rightarrow h_4 \rightarrow h_1 \rightarrow h_2 \rightarrow h_2 \rightarrow h_3 \rightarrow$

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Carry $h_0 \rightarrow h_1$: i.e., replace (h_0, h_1) with $(h_0 \mod 2^{26}, h_1 + \lfloor h_0/2^{26} \rfloor)$. This makes h_0 small.

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- Mix signed, unsigned carries.
- Interleave reduction, carrying.

Minor challenge: pipelining. Result of each insn cannot be used until a few cycles later.

Find an independent insn for the CPU to start working while the first insn is in programme.

Sometimes helps to adjust higher-level computations.

Example: carries $h_0 \rightarrow h_1 - h_2 \rightarrow h_3 \rightarrow h_4 \rightarrow h_5 \rightarrow h_6 - h_7 \rightarrow h_8 \rightarrow h_9 \rightarrow h_0 \rightarrow h_1$ have long chain of depender

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Carry $h_0 \rightarrow h_1$: i.e., replace (h_0, h_1) with $(h_0 \mod 2^{26}, h_1 + \lfloor h_0/2^{26} \rfloor)$. This makes h_0 small.

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ightarrow h_1$: i.e., h_0 , h_1) with $h_1
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for other h_i .

Ily all h_i are small enough.

ally use signed coeffs. more expensive carries etails of insn set) e room for $ab + c^2$ etc.

ings we haven't tried yet: gned, unsigned carries. ave reduction, carrying.

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 $h_4 \rightarrow h_5$

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Now muto for CPU

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h_i. re small enough.

gned coeffs. ensive carries sn set) $(ab + c^2)$ etc.

aven't tried yet: gned carries. tion, carrying. Minor challenge: pipelining. Result of each insn cannot be used until a few cycles later.

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12 carries instead but latency is much

 $h_5 \rightarrow h_6$ and h_0 —

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Minor challenge: pipelining. Result of each insn cannot be used until a few cycles later.

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Example: carries $h_0 \rightarrow h_1 \rightarrow h_2 \rightarrow h_3 \rightarrow h_4 \rightarrow h_5 \rightarrow h_6 \rightarrow h_7 \rightarrow h_8 \rightarrow h_9 \rightarrow h_0 \rightarrow h_1$ have long chain of dependencies. Alternative: carry

 $h_0 \rightarrow h_1$ and $h_5 \rightarrow h_6$; $h_1 \rightarrow h_2$ and $h_6 \rightarrow h_7$; $h_2 \rightarrow h_3$ and $h_7 \rightarrow h_8$; $h_3 \rightarrow h_4$ and $h_8 \rightarrow h_9$; $h_4 \rightarrow h_5$ and $h_9 \rightarrow h_0$; $h_5 \rightarrow h_6$ and $h_0 \rightarrow h_1$.

12 carries instead of 11, but latency is much smaller.

Now much easier to find independent insns for CPU to handle in paralle

Minor challenge: pipelining. Result of each insn cannot be used until a few cycles later.

Find an independent insn for the CPU to start working on while the first insn is in progress.

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Example: carries $h_0 \rightarrow h_1 \rightarrow h_2 \rightarrow h_3 \rightarrow h_4 \rightarrow h_5 \rightarrow h_6 \rightarrow h_7 \rightarrow h_8 \rightarrow h_9 \rightarrow h_0 \rightarrow h_1$ have long chain of dependencies. Alternative: carry

 $h_0 \rightarrow h_1$ and $h_5 \rightarrow h_6$; $h_1 \rightarrow h_2$ and $h_6 \rightarrow h_7$; $h_2 \rightarrow h_3$ and $h_7 \rightarrow h_8$; $h_3 \rightarrow h_4$ and $h_8 \rightarrow h_9$; $h_4 \rightarrow h_5$ and $h_9 \rightarrow h_0$; $h_5 \rightarrow h_6$ and $h_0 \rightarrow h_1$.

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hallenge: pipelining.

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e: carries $h_0 \rightarrow h_1 \rightarrow$ $\rightarrow h_4 \rightarrow h_5 \rightarrow h_6 \rightarrow$ $\rightarrow h_9 \rightarrow h_0 \rightarrow h_1$ g chain of dependencies. Alternative: carry $h_0 \rightarrow h_1$ and $h_5 \rightarrow h_6$; $h_1 \rightarrow h_2$ and $h_6 \rightarrow h_7$; $h_2 \rightarrow h_3$ and $h_7 \rightarrow h_8$; $h_3 \rightarrow h_4$ and $h_8 \rightarrow h_9$; $h_4 \rightarrow h_5$ and $h_9 \rightarrow h_0$; $h_5 \rightarrow h_6$ and $h_0 \rightarrow h_1$.

12 carries instead of 11, but latency is much smaller.

Now much easier to find independent insns for CPU to handle in parallel.

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 dependencies.

Alternative: carry

$$h_0 \rightarrow h_1$$
 and $h_5 \rightarrow h_6$;

$$h_1 \rightarrow h_2$$
 and $h_6 \rightarrow h_7$;

$$h_2 \rightarrow h_3$$
 and $h_7 \rightarrow h_8$;

$$h_3 \rightarrow h_4$$
 and $h_8 \rightarrow h_9$;

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Major challenge: vectorizati

e.g. 4x a = b + c does 4 additions at once, but needs particular arrange of inputs and outputs.

On Cortex-A8, occasional permutations run in parallel with arithmet but frequent permutations would be a bottleneck.

On Cortex-A7, every operation costs cycles.

 $h_0 \rightarrow h_1$ and $h_5 \rightarrow h_6$;

 $h_1 \rightarrow h_2$ and $h_6 \rightarrow h_7$;

 $h_2 \rightarrow h_3$ and $h_7 \rightarrow h_8$;

 $h_3 \rightarrow h_4$ and $h_8 \rightarrow h_9$;

 $h_4 \rightarrow h_5$ and $h_9 \rightarrow h_0$;

 $h_5 \rightarrow h_6$ and $h_0 \rightarrow h_1$.

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Merge f_0 and f_0 , f_0 into vectors

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 $\rightarrow h_6;$

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Often higher-level

Vectorize across the Merge f_0, f_1, \ldots, f_n and f'_0, f'_1, \ldots, f'_n into vectors (f_i, f'_i) . Similarly (g_i, g'_i) .

Then compute (h_i)

Computation fits rinto NEON insns: c[0,1] = a[0] si

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Vectorize across those mults

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Computation fits naturally into NEON insns: e.g., c[0,1] = a[0] signed* b[c[2,3] = a[1] signed* b[

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Example: Typical algorithms for fixed-base scalarmult have many parallel point adds.

gher-level operations r of mults in parallel: h' = f'g'.

e across those mults.

$$f_1, f_1, \dots, f_9$$

 f'_1, \dots, f'_9
 f'_1, \dots, f'_9
 f'_1, \dots, f'_1
 f'_1, \dots, f'_1

ation fits naturally

ON insns: e.g.,
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Beware a disadvantage of vectorizing across two mults: 256-bit f, f', g, g', h, h' occupy at least 1536 bits, leaving very little room for temporary registers.

We use some loads and stores inside vectorized mulmul.

Mostly invisible on Cortex-A8, but bigger issue on Cortex-A7.

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P, 5P, 6P, 7P as

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Some fie inside a

Example convert

$$Z^{-1}X \in$$

Easy, co
$$11M + 2$$

$$z2 = z1$$

$$z8 = z2$$

$$z9 = z1$$

$$z11 = z$$

$$z22 = z$$

$$z_5_0 =$$

 $Y_1 \cdot Y_2$ on formulas

npute 7*P* as

$$4P = 2P + 2P;$$

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Some field ops are inside a single scal

convert fraction ($Z^{-1}X \in \{0, 1, ...\}$

Example: At end

Easy, constant time 11M + 254S for p $z^2 = z^2^2$ z^2

z11 = z2*z9

z9 = z1*z8

 $z22 = z11^2^1$

 $z_5_0 = z_9*z_2$

 $z_10_5 = z_5_0^2$

as

+2P; +3P

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Some field ops are hard to principle a single scalarmult.

Example: At end of ECDH, convert fraction (X : Z) into $Z^{-1}X \in \{0, 1, ..., p-1\}.$

Easy, constant time: $Z^{-1} = 11$ M + 254**S** for $p = 2^{255}$ –

 $z2 = z1^2^1$

 $z8 = z2^2^2$

z9 = z1*z8

z11 = z2*z9

 $z22 = z11^2^1$

 $z_5_0 = z_9*z_22$

 $z_10_5 = z_5_0^25$

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z_10_0

$$z_{20_0} = 10^{-1}$$

$$z_{40_0} = 10^{-3}$$

$$z_{50_0} = 10^{-3}$$

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$$z_50_0 = z_50_10$$

$$z_100_50 = z_50_$$

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$$z_200_100 = z_10$$

$$z_200_0 = z_200_$$

$$z_250_50 = z_200$$

$$z_250_0 = z_250_$$

$$z_255_5 = z_250_$$

$$z_255_21 = z_255$$

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$$z_10_0 = z_10_5*z_5_0$$

$$z_20_10 = z_10_0^210$$

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$$z_100_50 = z_50_0^250$$

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nstant time: $Z^{-1} = Z^{p-2}$.

254**S** for $p = 2^{255} - 19$:

^2^1

^2^2

*z8

2*z9

11^2^1

z9*z22

 $= z_5_0^2$

 $z_10_0 = z_10_5*z_5_0$ $z_20_10 = z_10_0^210$ $z_20_0 = z_20_10*z_10_0$

 $z_40_20 = z_20_0^2$

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 $z_255_5 = z_250_0^25$

 $z_255_21 = z_255_5*z11$

Can still inside a

Strategy

50 mul i $(f_0, 2f_1), (f_2)$

 $(f_1, f_8), (f_3, f_8)$

 $(g_0,g_1),(g_2)$

 $(g_0, 19g_1), ($

 $(19g_2, 19g_3)$

 $(19g_2,g_3),($

Change e.g., (h_0) hard to pair larmult.

of ECDH, X:Z) into p-1.

ne:
$$Z^{-1} = Z^{p-2}$$
.
 $z = 2^{255} - 19$:

 $z_10_0 = z_10_5*z_5_0$ $z_20_10 = z_10_0^210$ $z_20_0 = z_20_10*z_10_0$ $z_40_20 = z_20_0^2$ $z_40_0 = z_40_20*z_20_0$ $z_50_10 = z_40_0^210$ $z_50_0 = z_50_10*z_10_0$ $z_100_50 = z_50_0^250$ $z_100_0 = z_100_50*z_50_0$ $z_200_100 = z_100_0^2100$ $z_200_0 = z_200_100*z_100_0$ $z_250_50 = z_200_0^250$ $z_250_0 = z_250_50*z_50_0$ $z_255_5 = z_250_0^25$ $z_255_21 = z_255_5*z11$

inside a single field Strategy in our so 50 mul insns start $(f_0,2f_1),(f_2,2f_3),(f_4,2f_5),$ $(f_1, f_8), (f_3, f_0), (f_5, f_2), (f_7, f_8)$ $(g_0,g_1),(g_2,g_3),(g_4,g_5),(g_5,g_5),(g_5$ $(g_0,19g_1),(g_2,19g_3),(g_4,$ $(19g_2, 19g_3), (19g_4, 19g_5)$ $(19g_2,g_3),(19g_4,g_5),(19g_4,g_5)$

Can still vectorize

Change carry patt e.g., $(h_0, h_4) \rightarrow (h_0, h_4)$

air

 Z^{p-2} .

19:

Can still vectorize inside a single field op.

Strategy in our software:

50 mul insns starting from $(f_0,2f_1),(f_2,2f_3),(f_4,2f_5),(f_6,2f_7),(f_8,2f_7),(f_1,f_8),(f_3,f_0),(f_5,f_2),(f_7,f_4),(f_9,f_6);$ $(g_0,g_1),(g_2,g_3),(g_4,g_5),(g_6,g_7);$ $(g_0,19g_1),(g_2,19g_3),(g_4,19g_5),(g_6,19g_6),(g_6,19g_7),(g_6,1$

Change carry pattern to vec e.g., $(h_0, h_4) \rightarrow (h_1, h_5)$.

 $(19g_2,g_3),(19g_4,g_5),(19g_6,g_7),(19g_8,g_7)$

 $z_10_0 = z_10_5*z_5_0$

 $z_20_10 = z_10_0^210$

 $z_20_0 = z_20_10*z_10_0$

 $z_40_20 = z_20_0^2$

 $z_40_0 = z_40_20*z_20_0$

 $z_50_10 = z_40_0^210$

 $z_50_0 = z_50_10*z_10_0$

 $z_100_50 = z_50_0^250$

 $z_100_0 = z_100_50*z_50_0$

 $z_200_100 = z_100_0^2100$

 $z_200_0 = z_200_100*z_100_0$

 $z_250_50 = z_200_0^250$

 $z_250_0 = z_250_50*z_50_0$

 $z_255_5 = z_250_0^25$

 $z_255_21 = z_255_5*z11$

Can still vectorize inside a single field op.

Strategy in our software:

50 mul insns starting from

 $(f_0,2f_1),(f_2,2f_3),(f_4,2f_5),(f_6,2f_7),(f_8,2f_9);$

 $(f_1, f_8), (f_3, f_0), (f_5, f_2), (f_7, f_4), (f_9, f_6);$

 $(g_0,g_1),(g_2,g_3),(g_4,g_5),(g_6,g_7);$

 $(g_0,19g_1),(g_2,19g_3),(g_4,19g_5),(g_6,19g_7),(g_8,19g_9);$

 $(19g_{2},19g_{3}),(19g_{4},19g_{5}),(19g_{6},19g_{7}),(19g_{8},19g_{9});$

 $(19g_{2},g_{3}),(19g_{4},g_{5}),(19g_{6},g_{7}),(19g_{8},g_{9}).$

Change carry pattern to vectorize, e.g., $(h_0, h_4) \rightarrow (h_1, h_5)$.

 $= z_10_5*z_5_0$ $= z_10_0^210$ $= z_20_10*z_10_0$ $= z_20_0^2$ $= z_40_20*z_20_0$

 $= z_50_10*z_10_0$

 $= z_40_0^210$

 $0 = z_50_0^250$ $= z_100_50*z_50_0$

 $00 = z_100_0^2100$

 $= z_200_100*z_100_0$

 $0 = z_200_0^250$

 $= z_250_50*z_50_0$

 $= z_250_0^25$

 $1 = z_255_5*z11$

Can still vectorize inside a single field op.

Strategy in our software:

50 mul insns starting from

 $(f_0,2f_1),(f_2,2f_3),(f_4,2f_5),(f_6,2f_7),(f_8,2f_9);$

 $(f_1, f_8), (f_3, f_0), (f_5, f_2), (f_7, f_4), (f_9, f_6);$

 $(g_0,g_1),(g_2,g_3),(g_4,g_5),(g_6,g_7);$

 $(g_0,19g_1),(g_2,19g_3),(g_4,19g_5),(g_6,19g_7),(g_8,19g_9);$

 $(19g_2,19g_3),(19g_4,19g_5),(19g_6,19g_7),(19g_8,19g_9);$

 $(19g_2,g_3),(19g_4,g_5),(19g_6,g_7),(19g_8,g_9).$

Change carry pattern to vectorize, e.g., $(h_0, h_4) \rightarrow (h_1, h_5)$.

on mul i Squaring

Core arit

Some lo

ECDH:

More de 356019 \approx 78% o

Cortex-A

Still som

z_5_0 ^2^10 *z_10_0 ^2^20 *z_20_0 ^2^10 *z_10_0 0^2^50 50*z_50_0 0_0^2^100

100*z_100_0 _0^2^50 50*z_50_0

0^2^5

_5*z11

Can still vectorize inside a single field op.

Strategy in our software:

50 mul insns starting from

$$(f_0,2f_1),(f_2,2f_3),(f_4,2f_5),(f_6,2f_7),(f_8,2f_9);$$

 $(f_1,f_8),(f_3,f_0),(f_5,f_2),(f_7,f_4),(f_9,f_6);$
 $(g_0,g_1),(g_2,g_3),(g_4,g_5),(g_6,g_7);$
 $(g_0,19g_1),(g_2,19g_3),(g_4,19g_5),(g_6,19g_7),(g_8,19g_9);$
 $(19g_2,19g_3),(19g_4,19g_5),(19g_6,19g_7),(19g_8,19g_9);$
 $(19g_2,g_3),(19g_4,g_5),(19g_6,g_7),(19g_8,g_9).$

Change carry pattern to vectorize, e.g., $(h_0, h_4) \rightarrow (h_1, h_5)$.

Core arithmetic: 1 on mul insns for earlings are som

Some loss for carr

ECDH: \approx 10 field

More detailed ana 356019 cycles on a $\approx 78\%$ of software Cortex-A8-fast cycles Still some room for

Can still vectorize inside a single field op.

Strategy in our software:

50 mul insns starting from

$$(f_0,2f_1),(f_2,2f_3),(f_4,2f_5),(f_6,2f_7),(f_8,2f_9);$$

 $(f_1,f_8),(f_3,f_0),(f_5,f_2),(f_7,f_4),(f_9,f_6);$
 $(g_0,g_1),(g_2,g_3),(g_4,g_5),(g_6,g_7);$
 $(g_0,19g_1),(g_2,19g_3),(g_4,19g_5),(g_6,19g_7),(g_8,19g_9);$
 $(19g_2,19g_3),(19g_4,19g_5),(19g_6,19g_7),(19g_8,19g_9);$
 $(19g_2,g_3),(19g_4,g_5),(19g_6,g_7),(19g_8,g_9).$

Change carry pattern to vectorize, e.g., $(h_0, h_4) \rightarrow (h_1, h_5)$.

Core arithmetic: 100 cycles on mul insns for each field resonantings are somewhat fast

Some loss for carries etc.

ECDH: \approx 10 field muls · 255

More detailed analysis: 356019 cycles on arithmetic ≈78% of software's total Cortex-A8-fast cycles for EC Still some room for improve

Can still vectorize inside a single field op.

Strategy in our software:

50 mul insns starting from

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 $(f_1,f_8),(f_3,f_0),(f_5,f_2),(f_7,f_4),(f_9,f_6);$
 $(g_0,g_1),(g_2,g_3),(g_4,g_5),(g_6,g_7);$
 $(g_0,19g_1),(g_2,19g_3),(g_4,19g_5),(g_6,19g_7),(g_8,19g_9);$
 $(19g_2,19g_3),(19g_4,19g_5),(19g_6,19g_7),(19g_8,19g_9);$
 $(19g_2,g_3),(19g_4,g_5),(19g_6,g_7),(19g_8,g_9).$

Change carry pattern to vectorize, e.g., $(h_0, h_4) \rightarrow (h_1, h_5)$.

Core arithmetic: 100 cycles on mul insns for each field mul. Squarings are somewhat faster.

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Strategy in our software:

50 mul insns starting from

$$(f_0,2f_1),(f_2,2f_3),(f_4,2f_5),(f_6,2f_7),(f_8,2f_9);$$

 $(f_1,f_8),(f_3,f_0),(f_5,f_2),(f_7,f_4),(f_9,f_6);$
 $(g_0,g_1),(g_2,g_3),(g_4,g_5),(g_6,g_7);$
 $(g_0,19g_1),(g_2,19g_3),(g_4,19g_5),(g_6,19g_7),(g_8,19g_9);$
 $(19g_2,19g_3),(19g_4,19g_5),(19g_6,19g_7),(19g_8,19g_9);$
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Each CPU is a new adventure.

e.g. Could it be better to use

Cortex-A7 FPU with radix 2^{21.25}?

vectorize single field op.

in our software:

nsns starting from

$$(2f_3), (f_4, 2f_5), (f_6, 2f_7), (f_8, 2f_9);$$

$$(f_0), (f_5, f_2), (f_7, f_4), (f_9, f_6);$$

$$(g_{3}),(g_{4},g_{5}),(g_{6},g_{7});$$

$$g_2, 19g_3), (g_4, 19g_5), (g_6, 19g_7), (g_8, 19g_9);$$

$$(19g_4, 19g_5), (19g_6, 19g_7), (19g_8, 19g_9);$$

$$19g_4,g_5),(19g_6,g_7),(19g_8,g_9).$$

carry pattern to vectorize, $(h_4) \rightarrow (h_1, h_5)$.

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Much m

https://benchma 2137 pu hundreds 39 DH p 56 signa

304 auth

ftware:

ing from

$$(f_6, 2f_7), (f_8, 2f_9);$$

$$f_4$$
), (f_9,f_6) ;

$$19g_5$$
), $(g_6,19g_7)$, $(g_8,19g_9)$;

$$(19g_6, 19g_7), (19g_8, 19g_9);$$

$$(6,g_7),(19g_8,g_9).$$

ern to vectorize, h_1, h_5).

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Much more work t

https://bench.dbenchmarks for (c 2137 public impler hundreds of crypto 39 DH primitives, 56 signature primi 304 authenticated 5);
7),(g₈,19g₉);
19g₈,19g₉);
9).

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Much more work to do

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Many interesting primitives are far slower than necessary on many important CPUs.

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Exercise: Make them faster!