The death of optimizing compilers

Daniel J. Bernstein University of Illinois at Chicago & Technische Universiteit Eindhoven

Programmers waste enormous amounts of time thinking about, or worrying about, the speed of noncritical parts of their programs, and these attempts at efficiency actually have a strong negative impact when debugging and maintenance are considered. We should forget about small efficiencies, say about 97% of the time; premature optimization is the root of all evil. (Donald E. Knuth,

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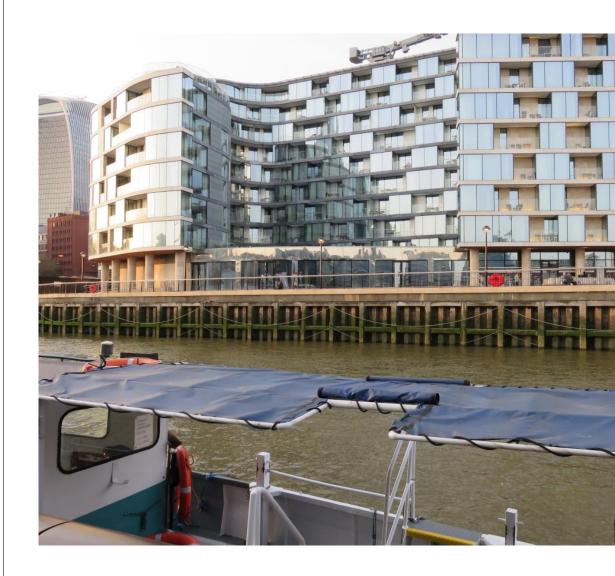
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Example: In your favorite sword-fighting video game, are light reflections affected realistically by sword vibration?



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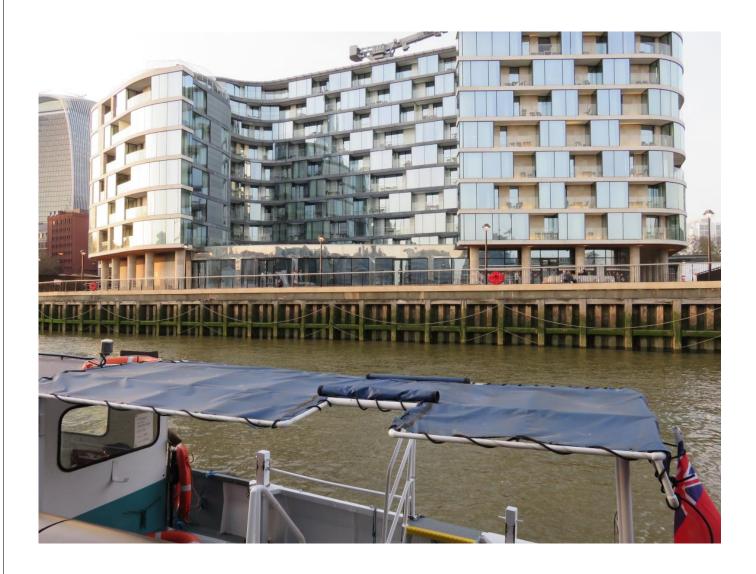
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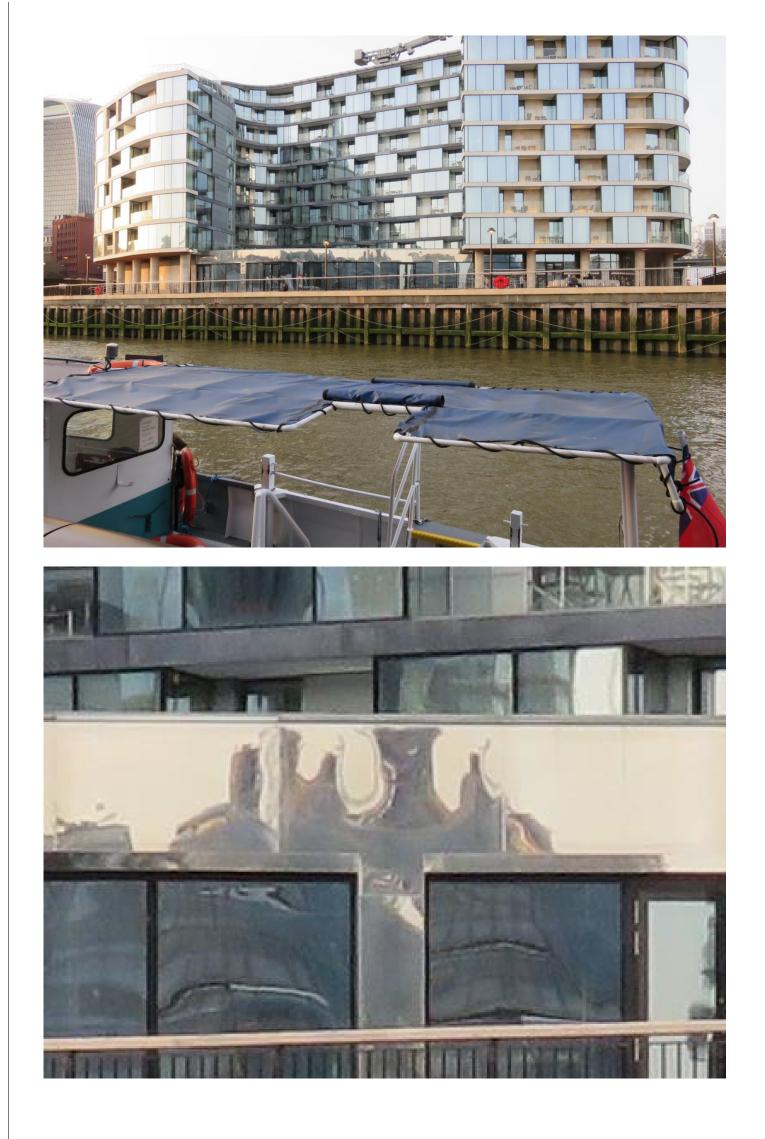
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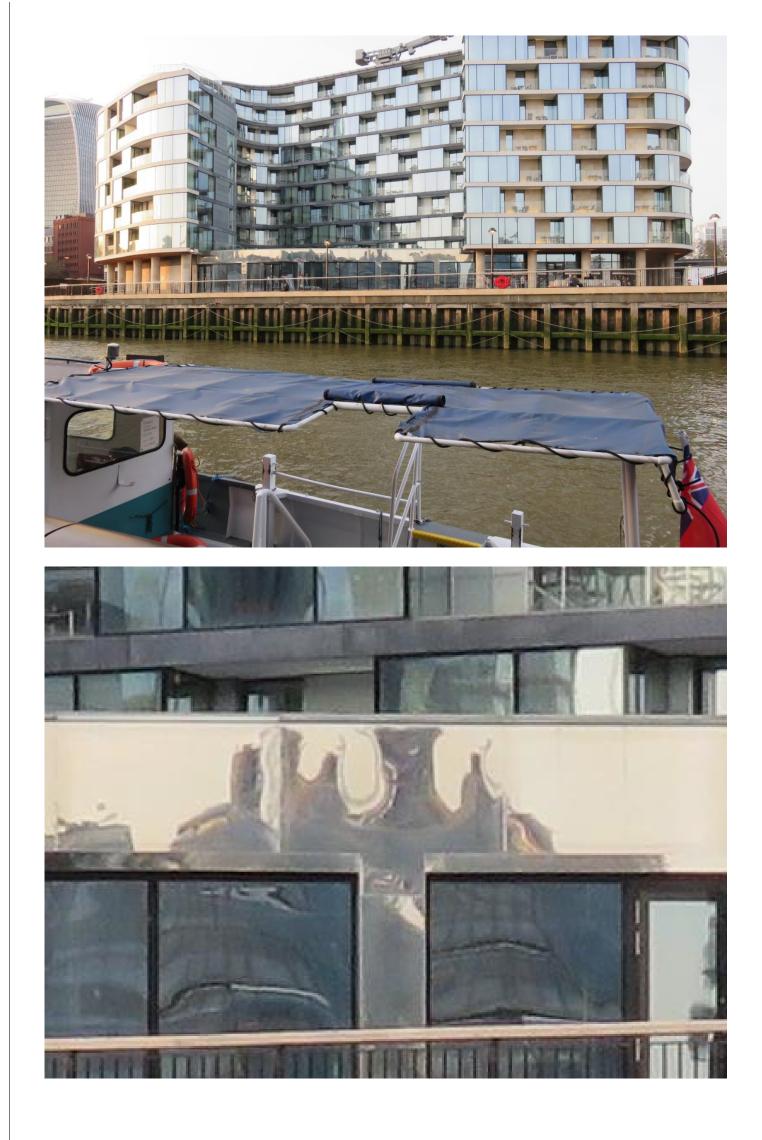
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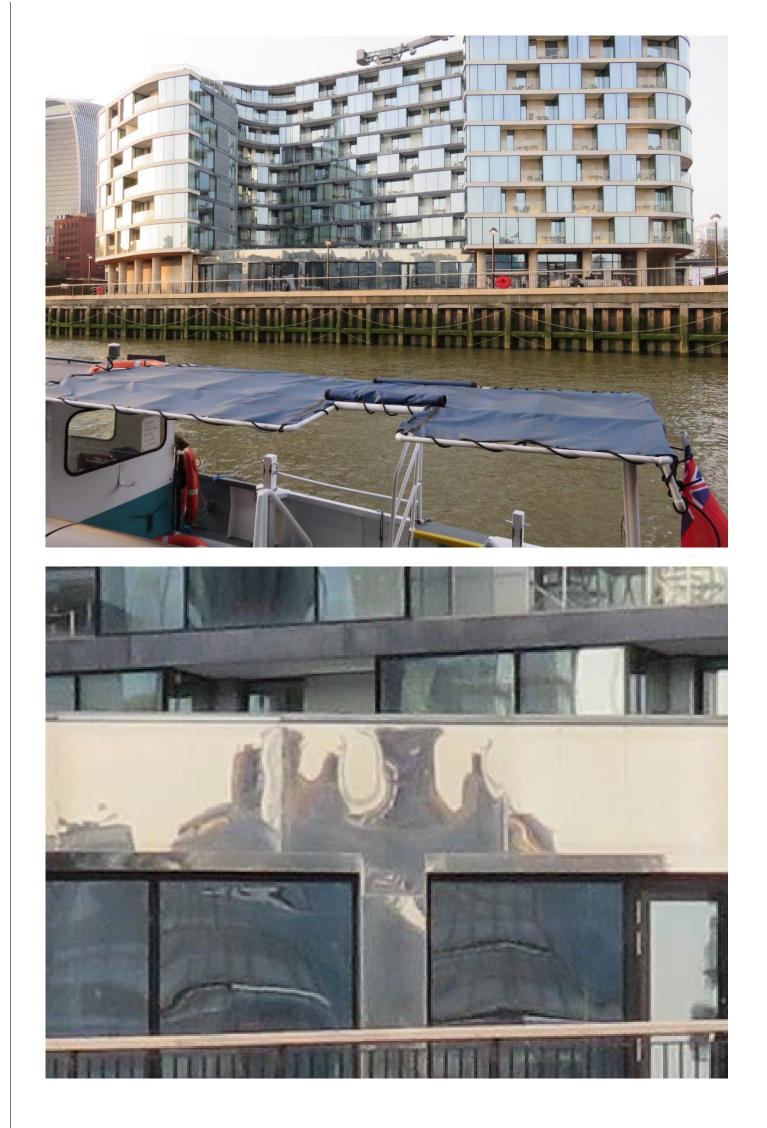
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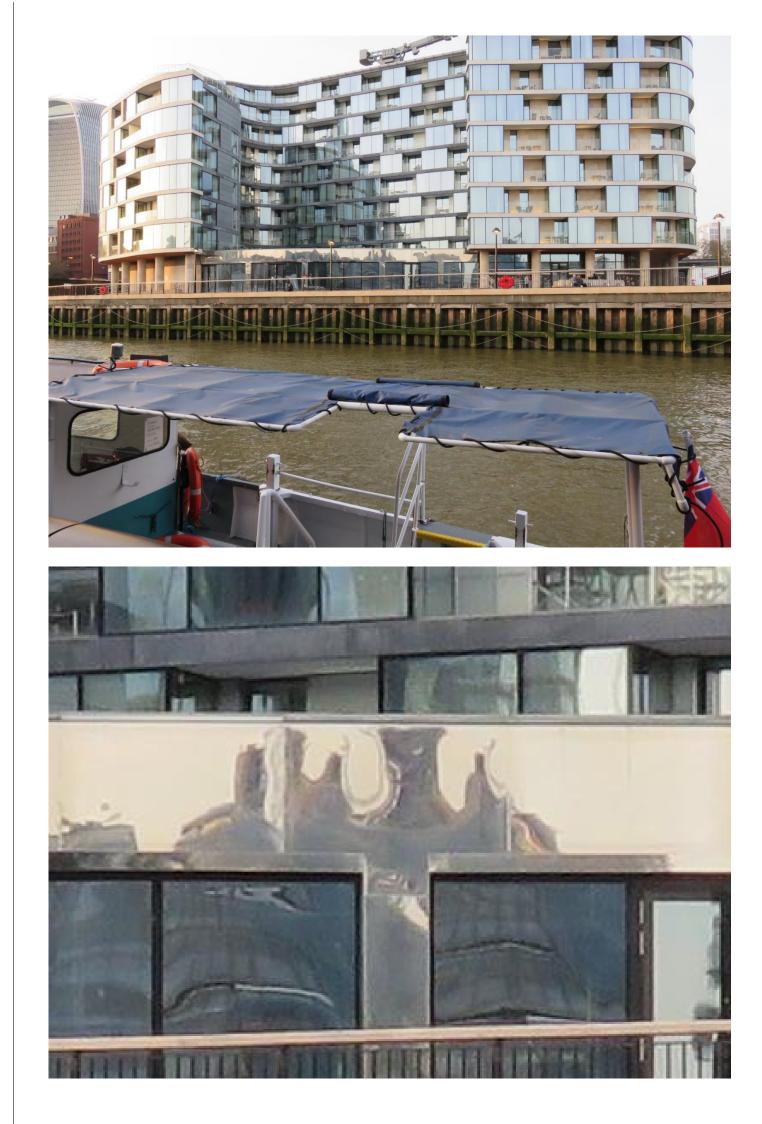


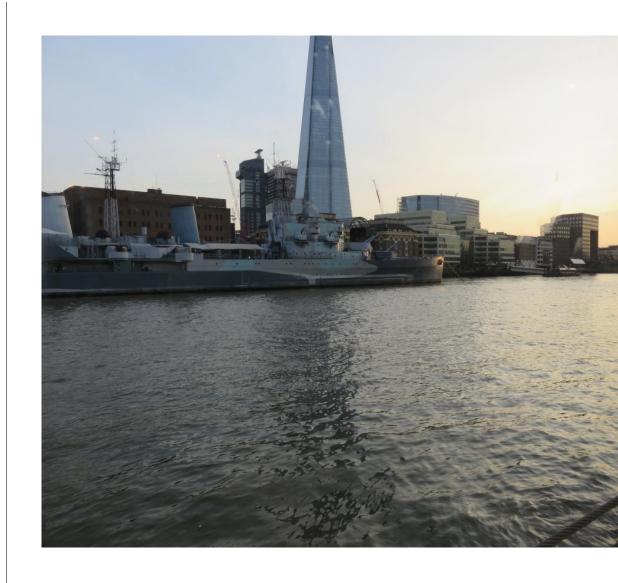


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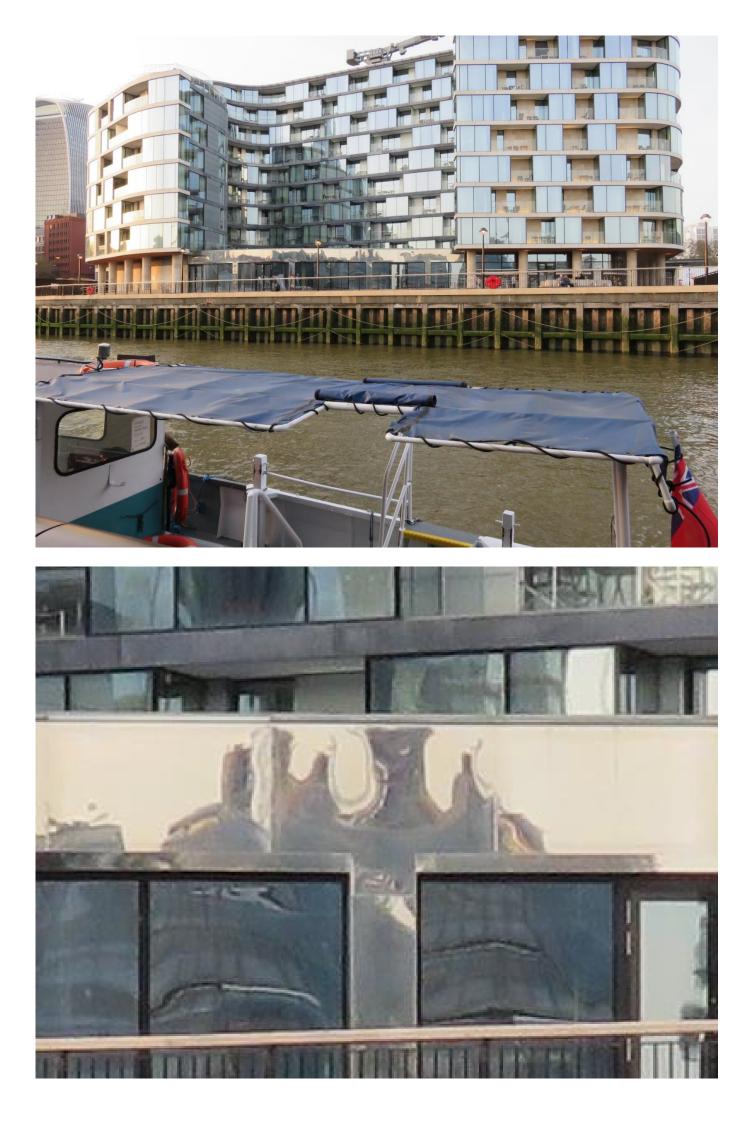


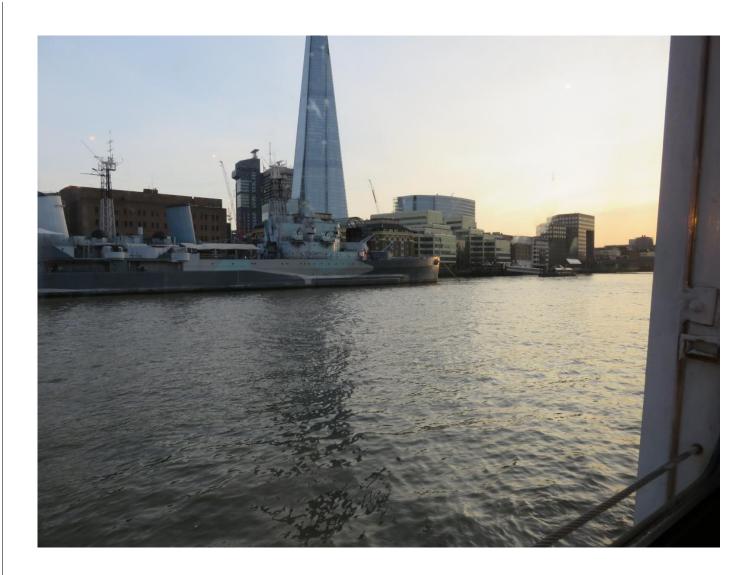


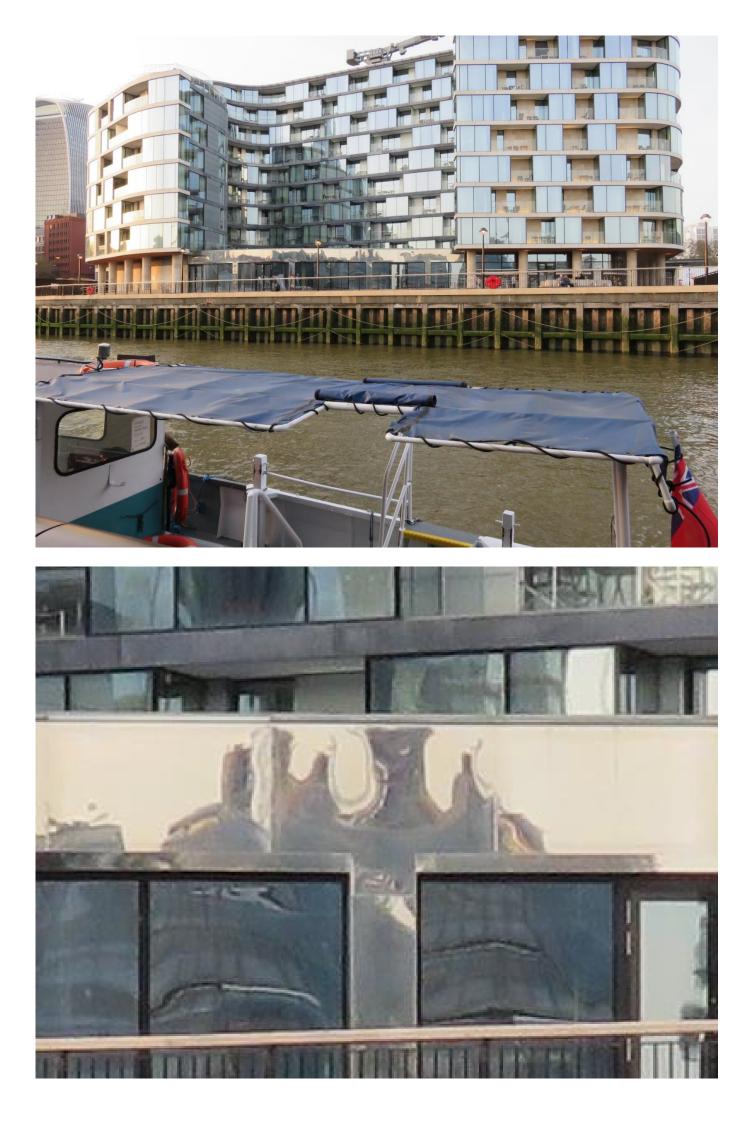


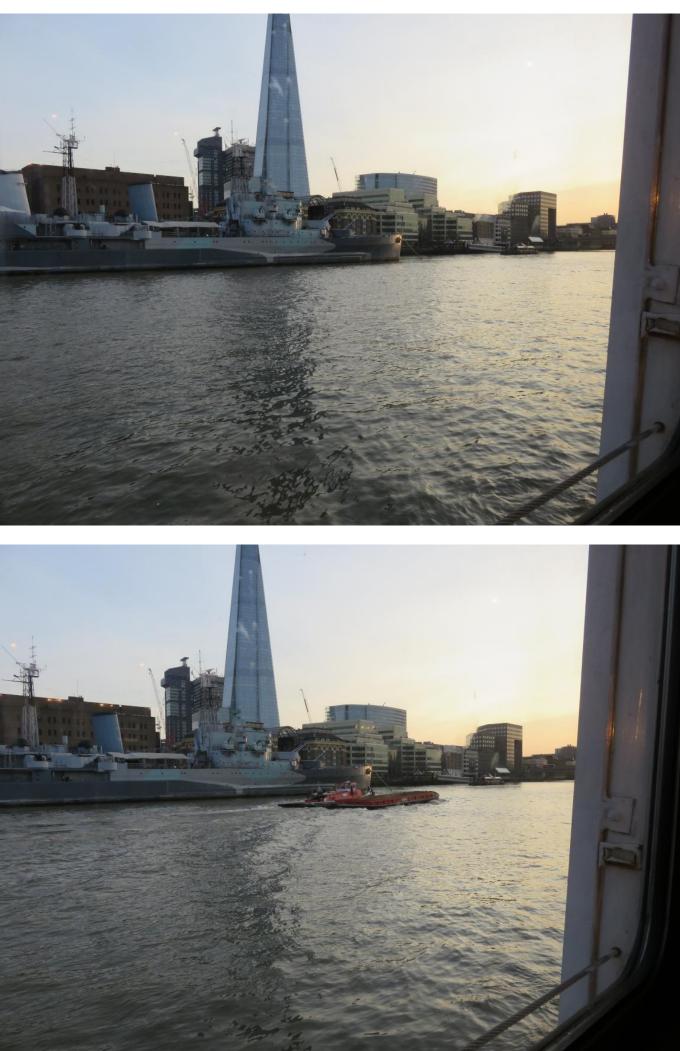
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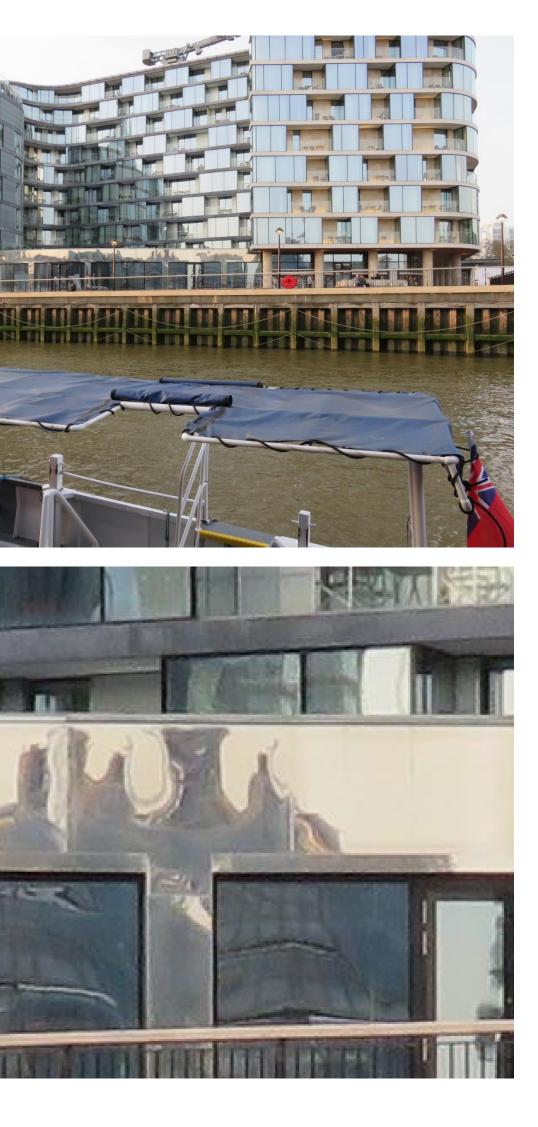
















Old CPL

0ms: St

400ms:

1200ms:

1600ms:







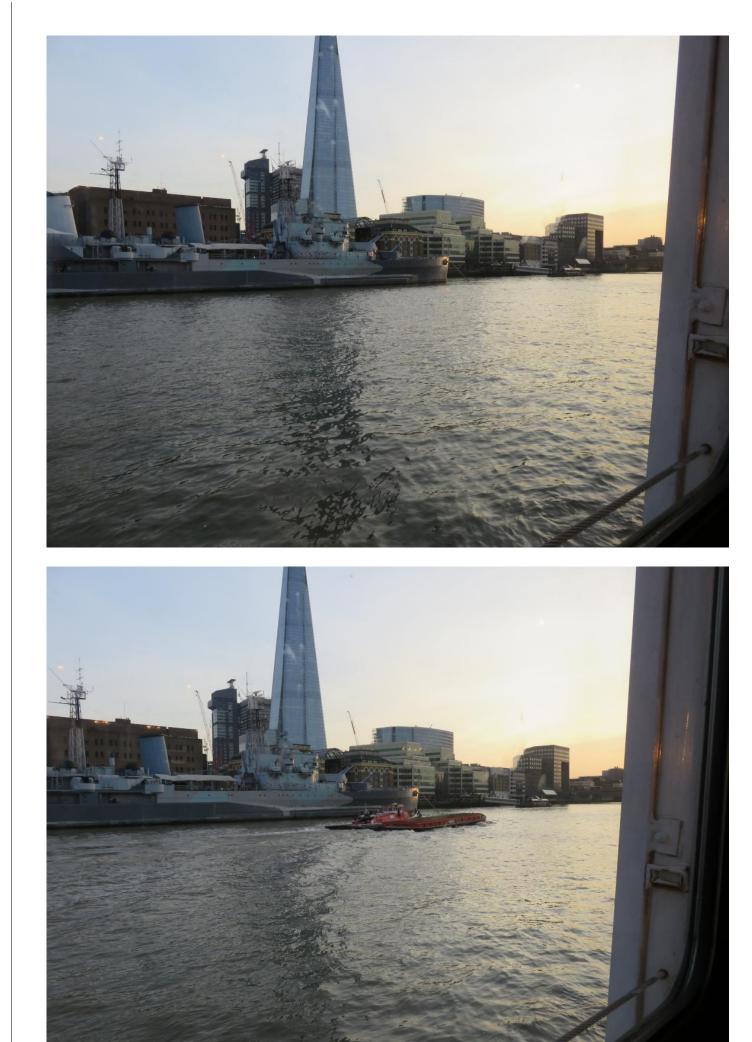
Old CPU displayin

Oms: Start openin

400ms: Start disp

1200ms: Start clea





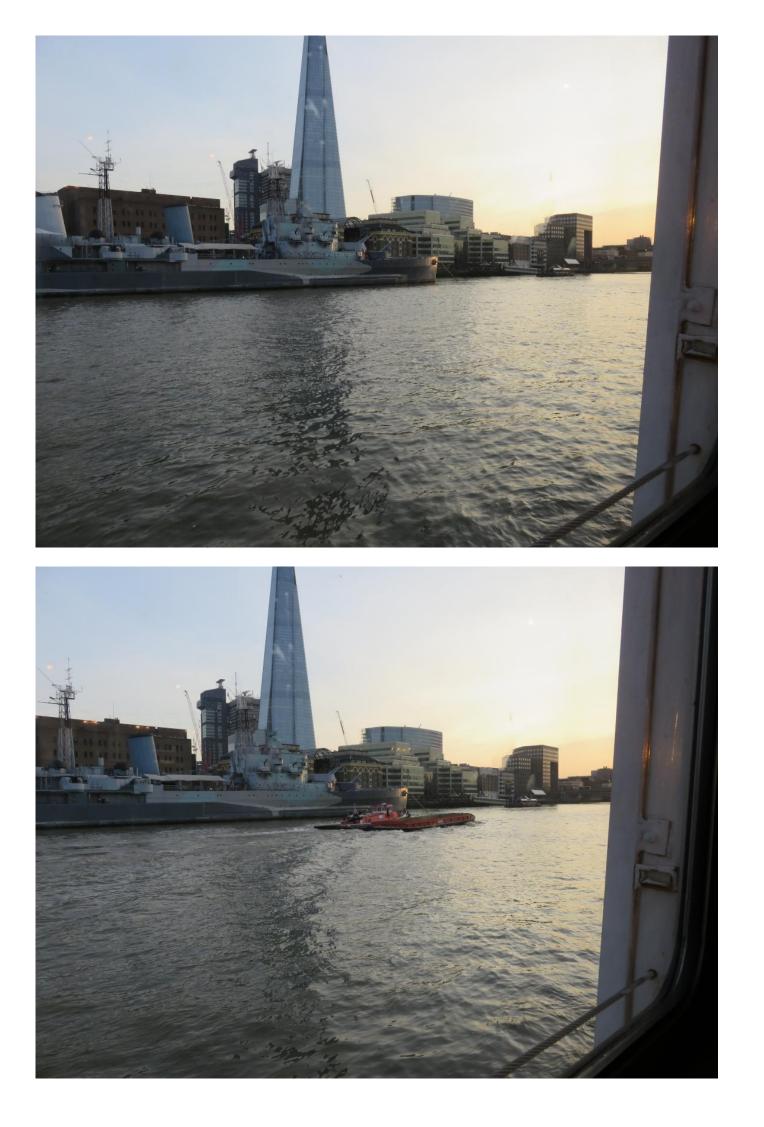
1600ms: Finish.

Old CPU displaying a file:

Oms: Start opening file.

400ms: Start displaying con

1200ms: Start cleaning up.

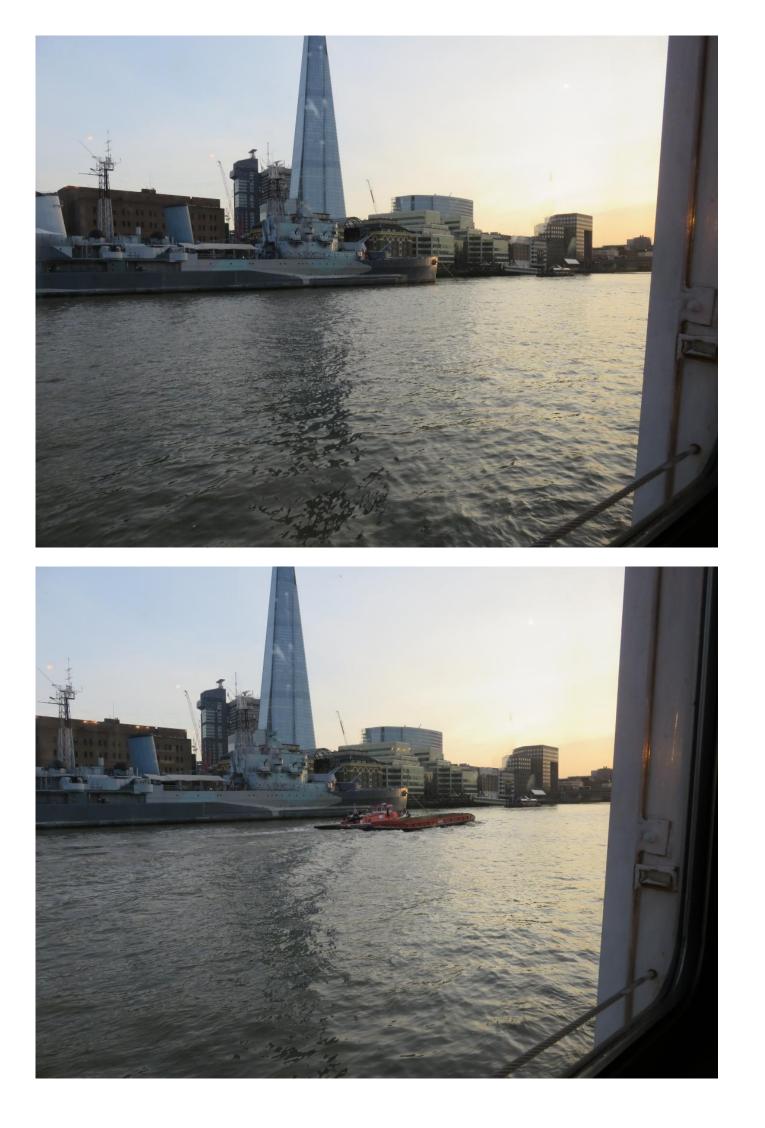


Old CPU displaying a file:

Oms: Start opening file.

400ms: Start displaying contents.

1200ms: Start cleaning up.

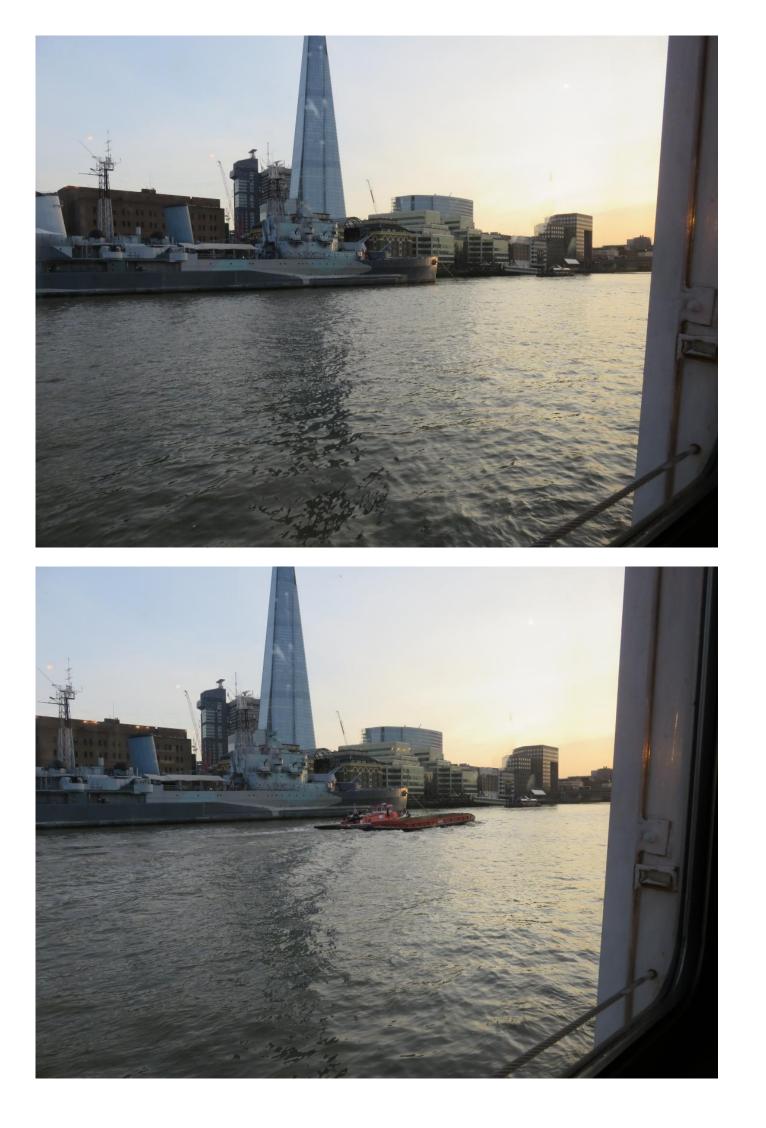


Oms: Start opening file.

1050ms: Start cleaning up.

1400ms: Finish.

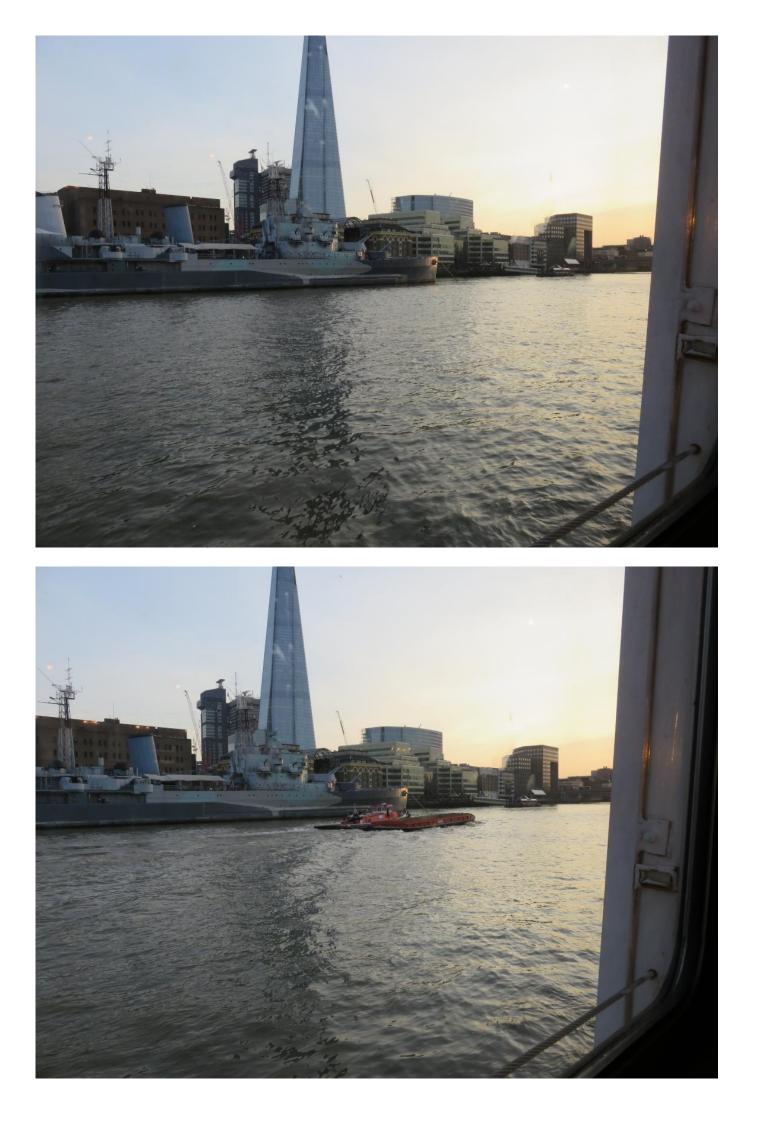
350ms: Start displaying contents.



Oms: Start opening file.

300ms: Start displaying contents.

900ms: Start cleaning up.

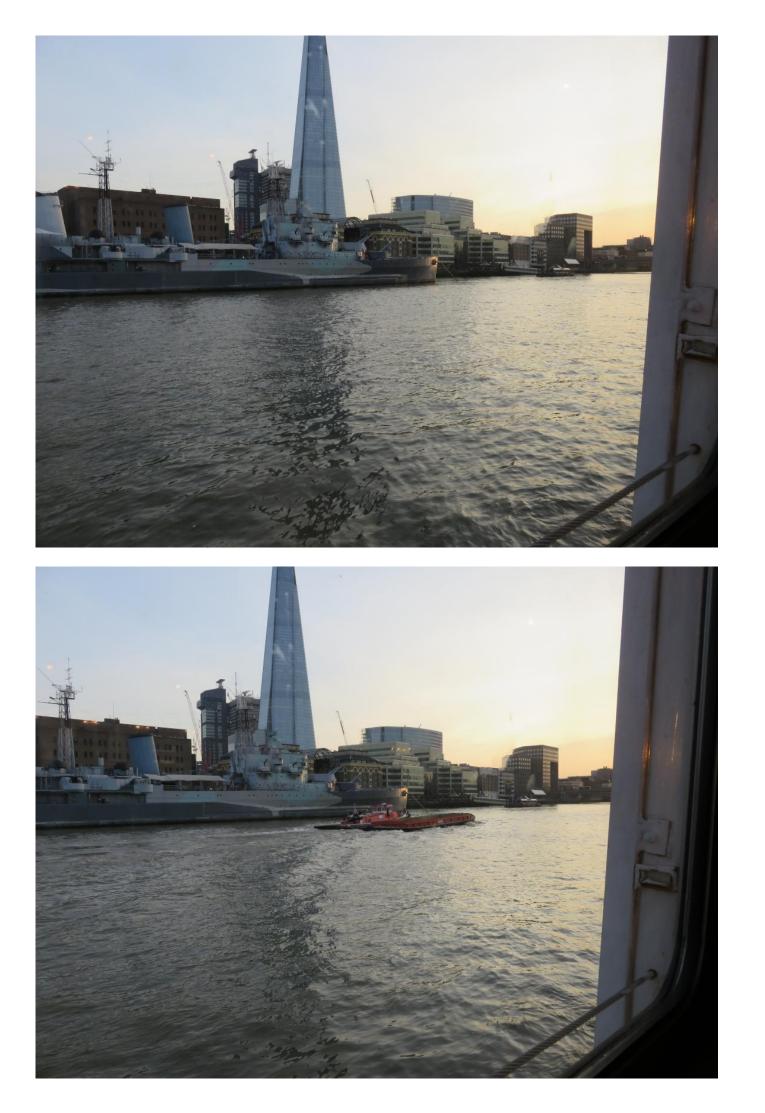


Oms: Start opening file.

800ms: Start cleaning up.

1000ms: Finish.

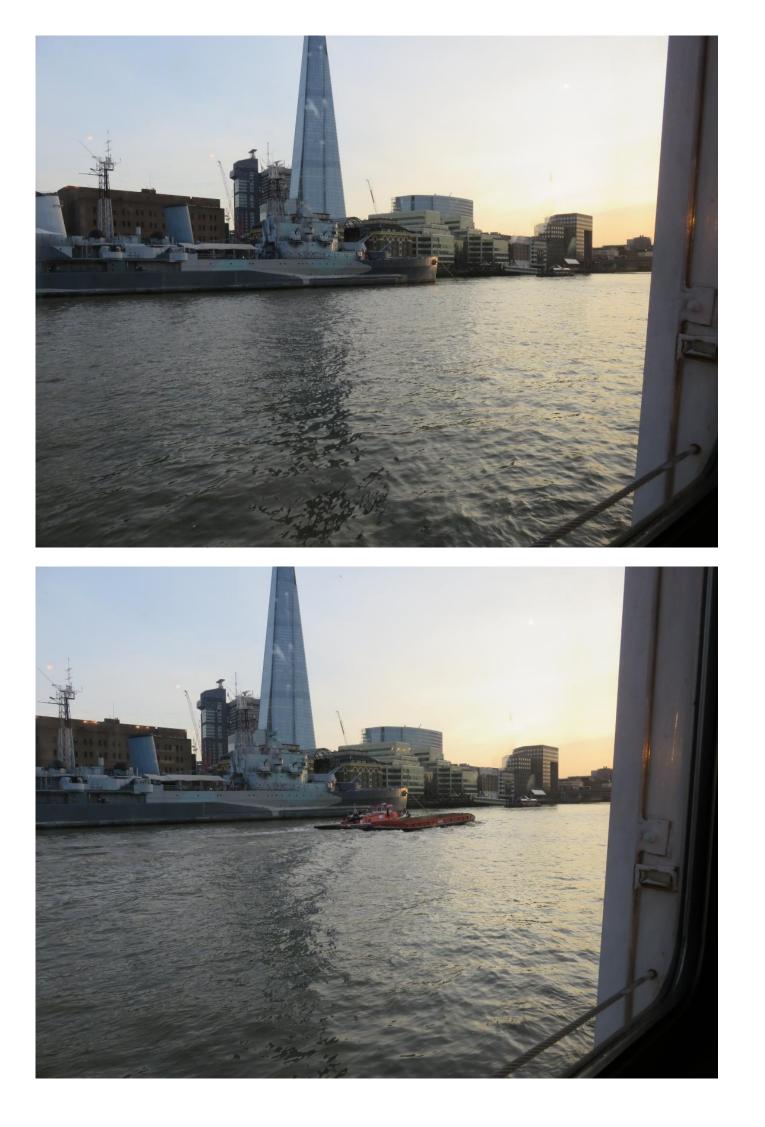
250ms: Start displaying contents.



Oms: Start opening file.

200ms: Start displaying contents.

600ms: Start cleaning up.

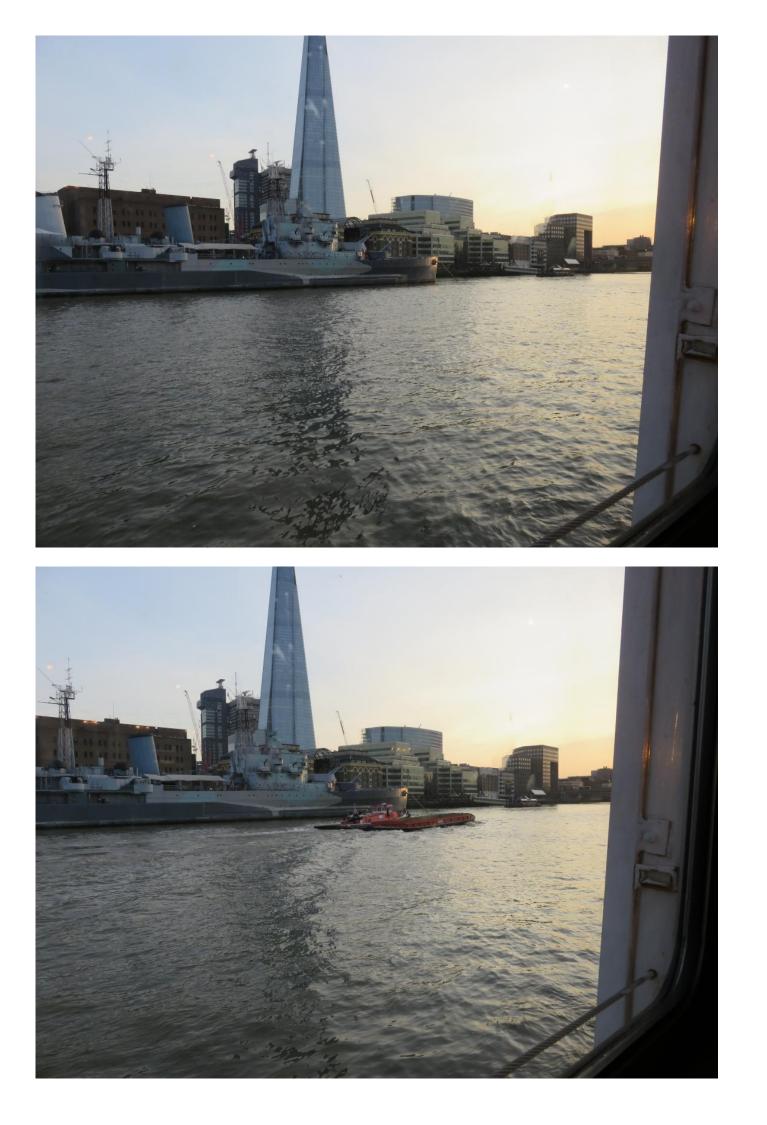


User displays bigger file:

Oms: Start opening file.

200ms: Start displaying contents.

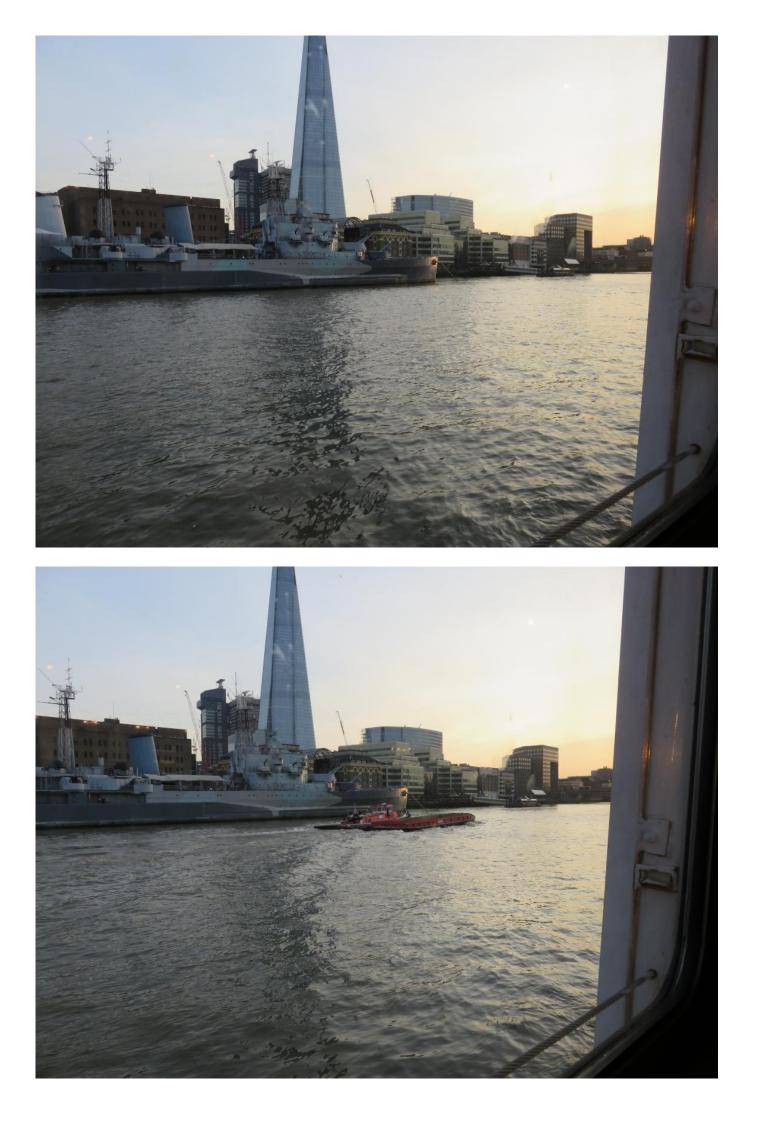
1000ms: Start cleaning up.



Oms: Start opening file.

175ms: Start displaying contents.

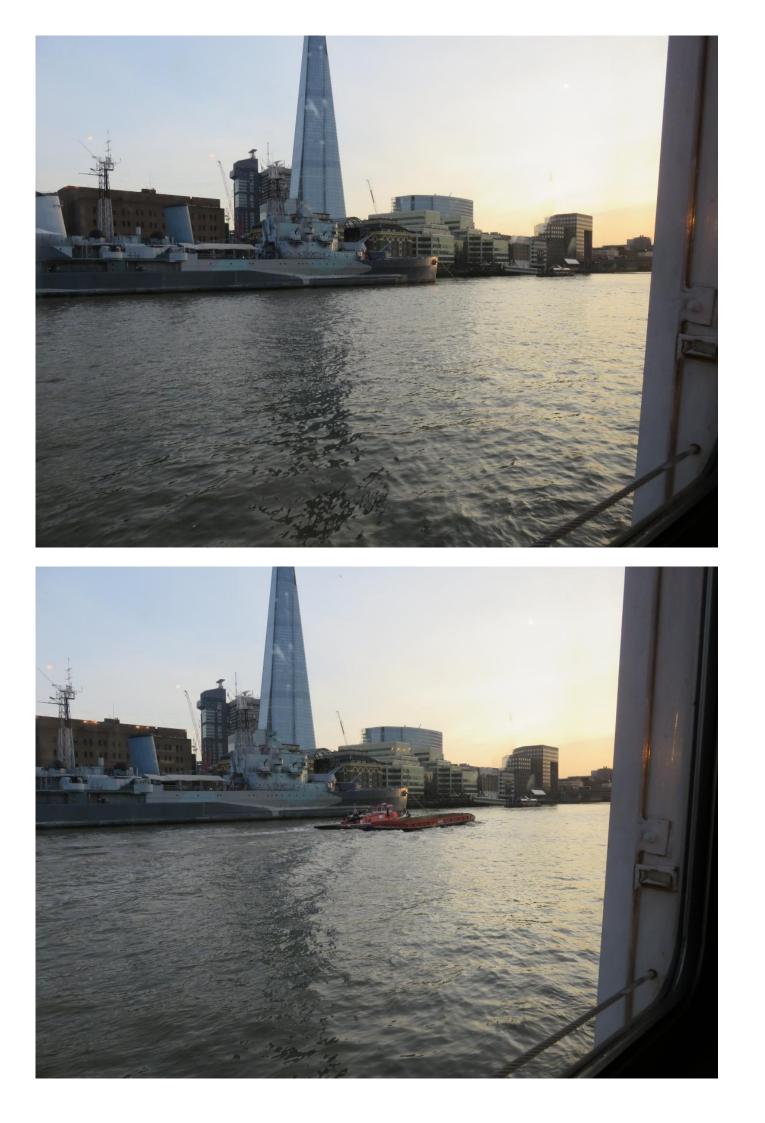
875ms: Start cleaning up.



Oms: Start opening file.

750ms: Start cleaning up. 900ms: Finish.

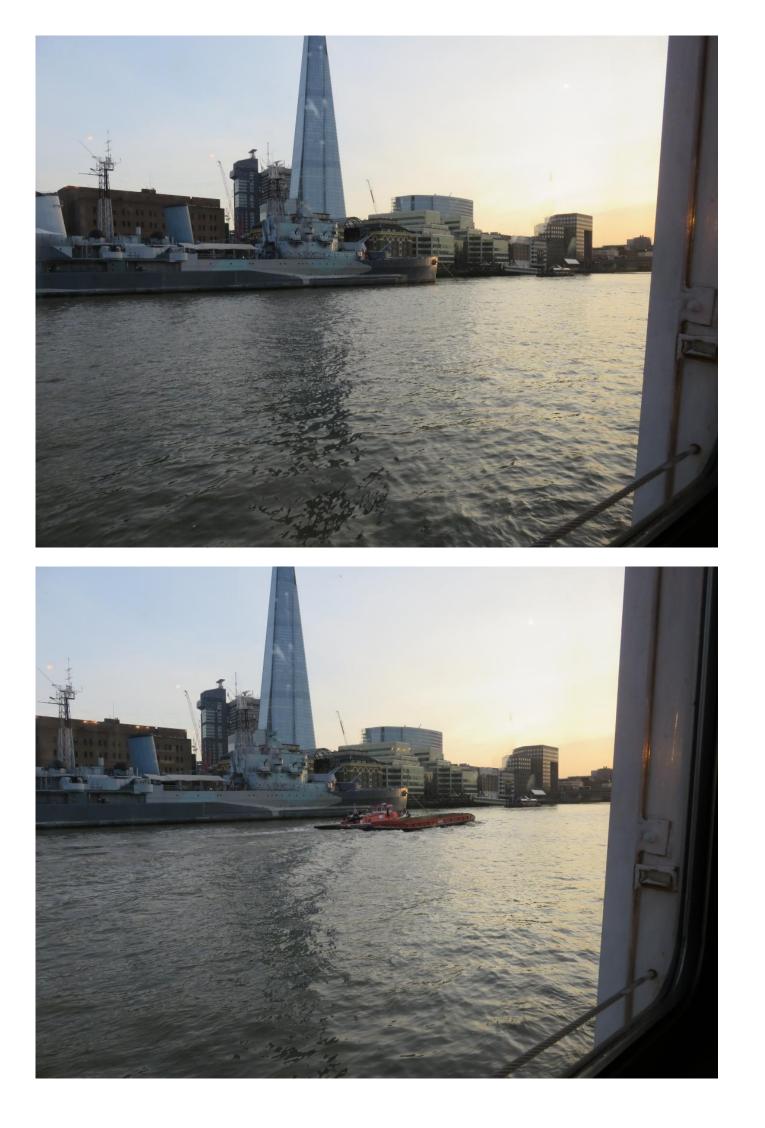
150ms: Start displaying contents.



Oms: Start opening file.

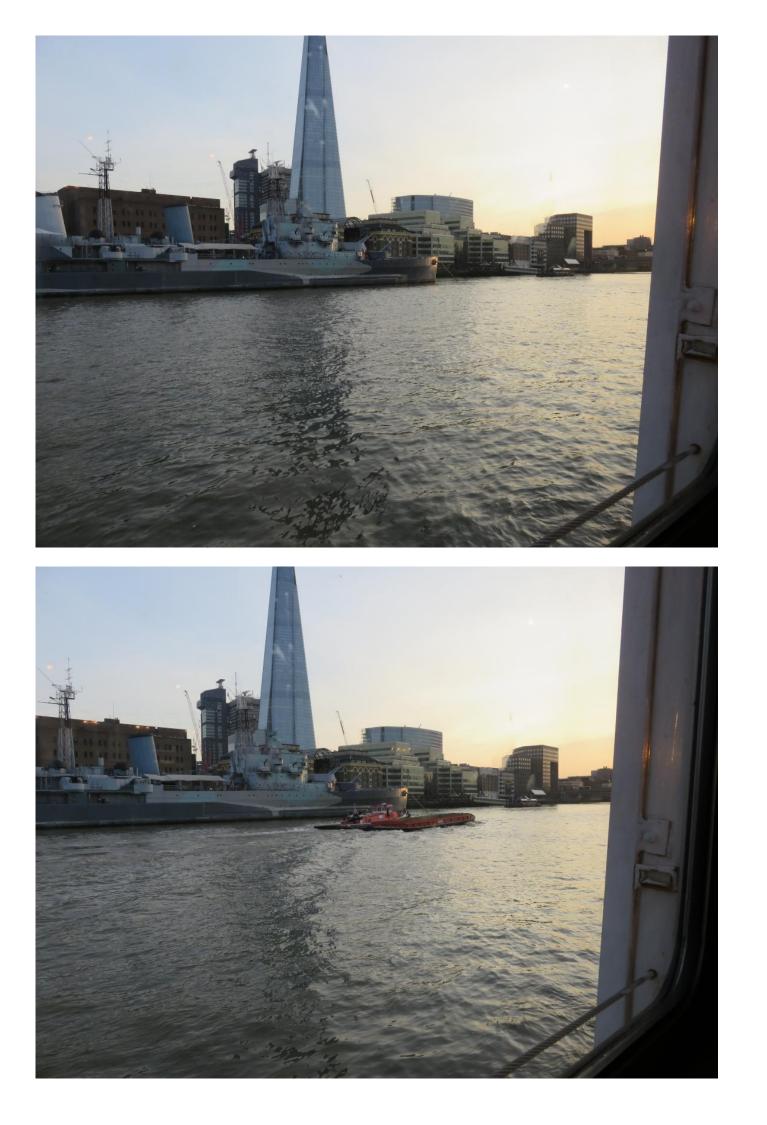
625ms: Start cleaning up. 750ms: Finish.

125ms: Start displaying contents.



Oms: Start opening file. 100ms: Start displaying contents.

500ms: Start cleaning up. 600ms: Finish.

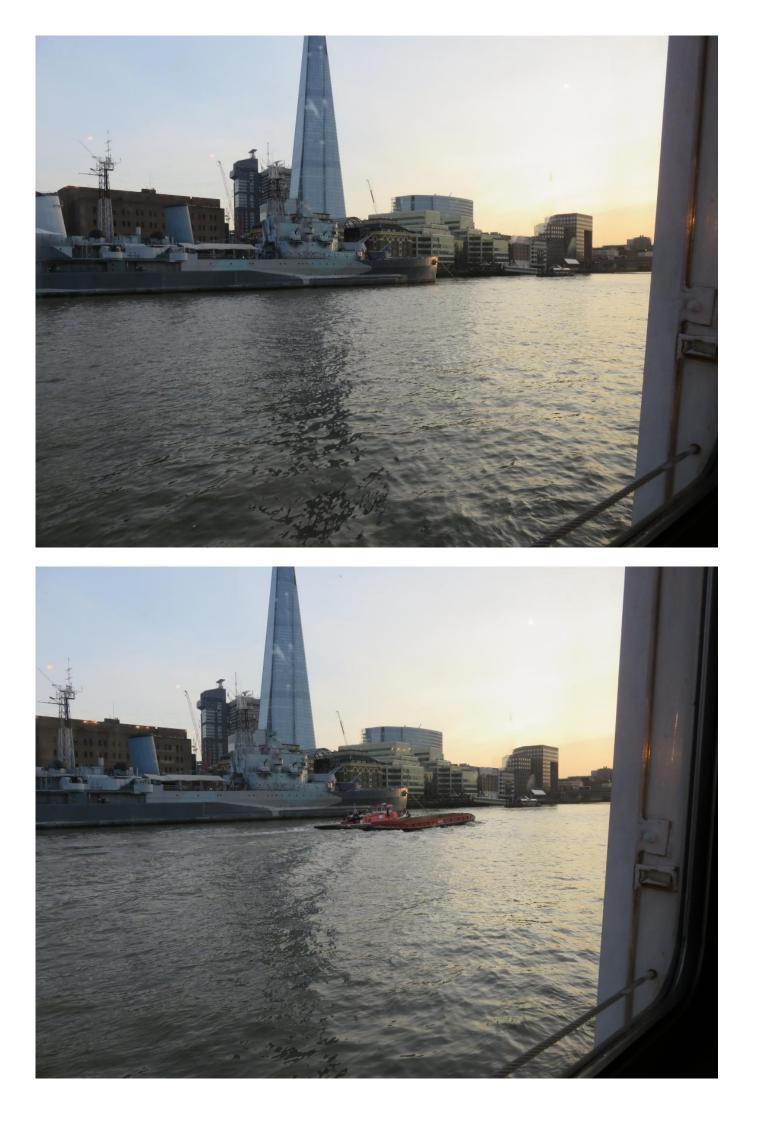


User displays bigger file:

Oms: Start opening file.

900ms: Start cleaning up. 1000ms: Finish.

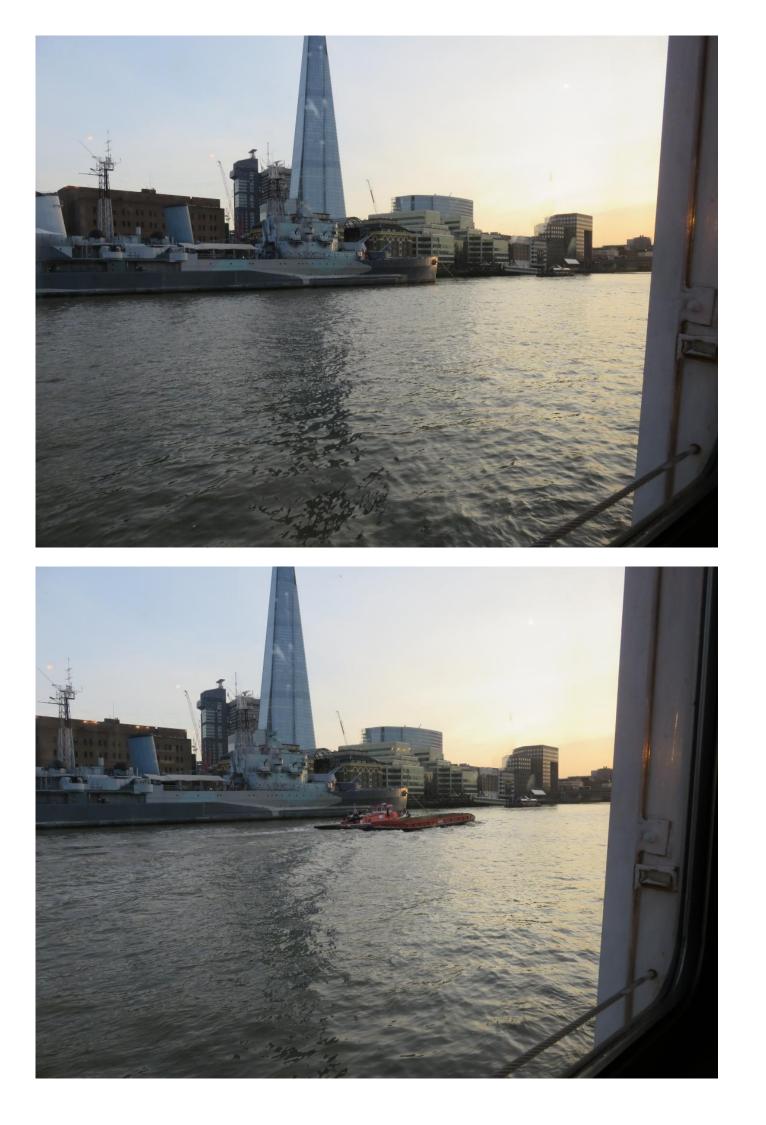
100ms: Start displaying contents.



1000ms: Finish.

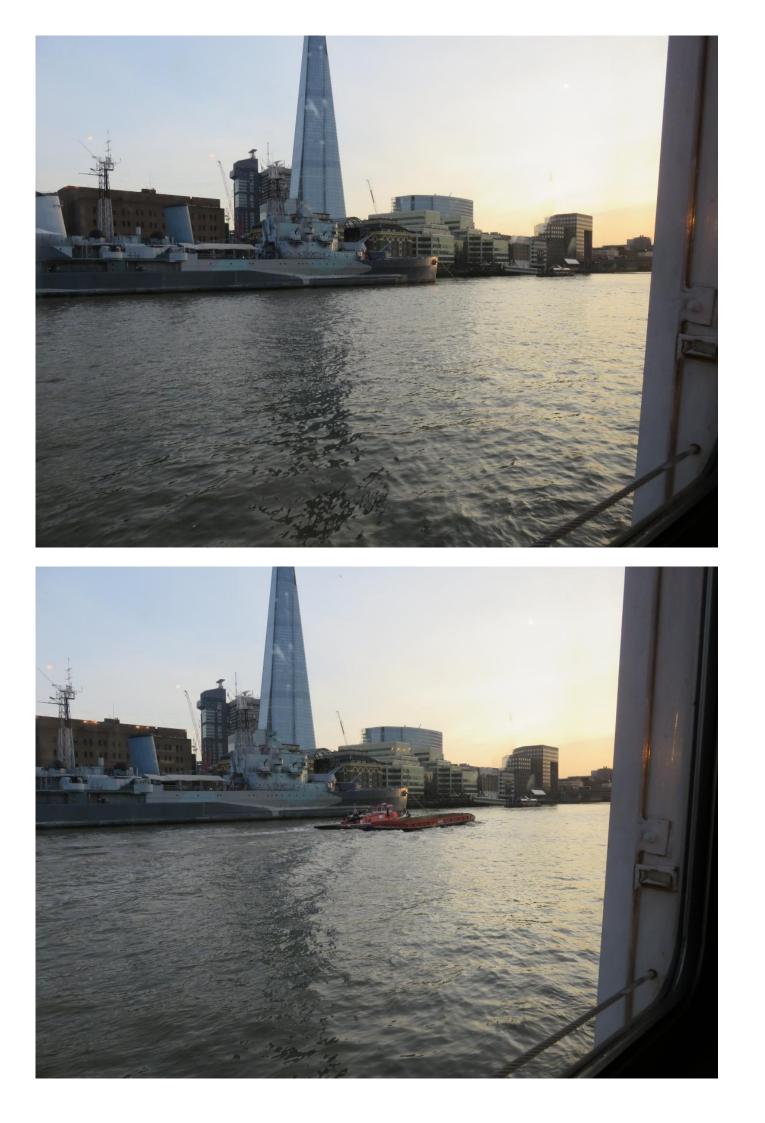


100ms: Start displaying contents.



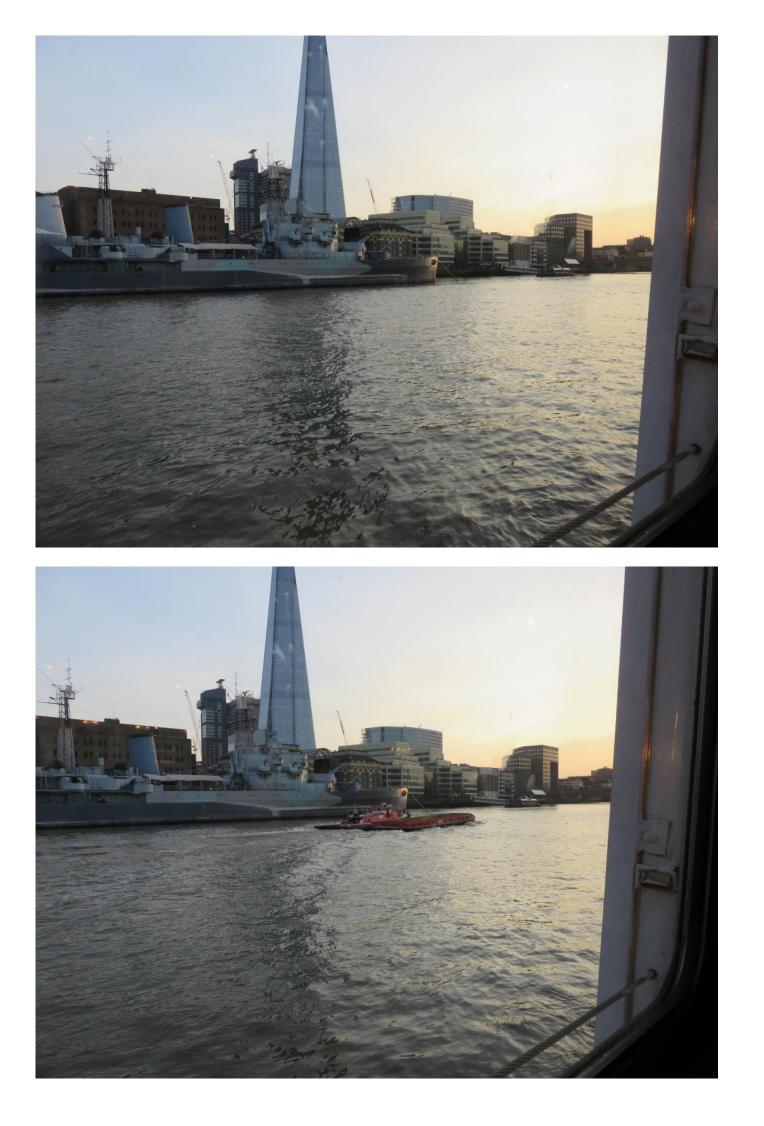
875ms: Finish.

87.5ms: Start displaying contents.



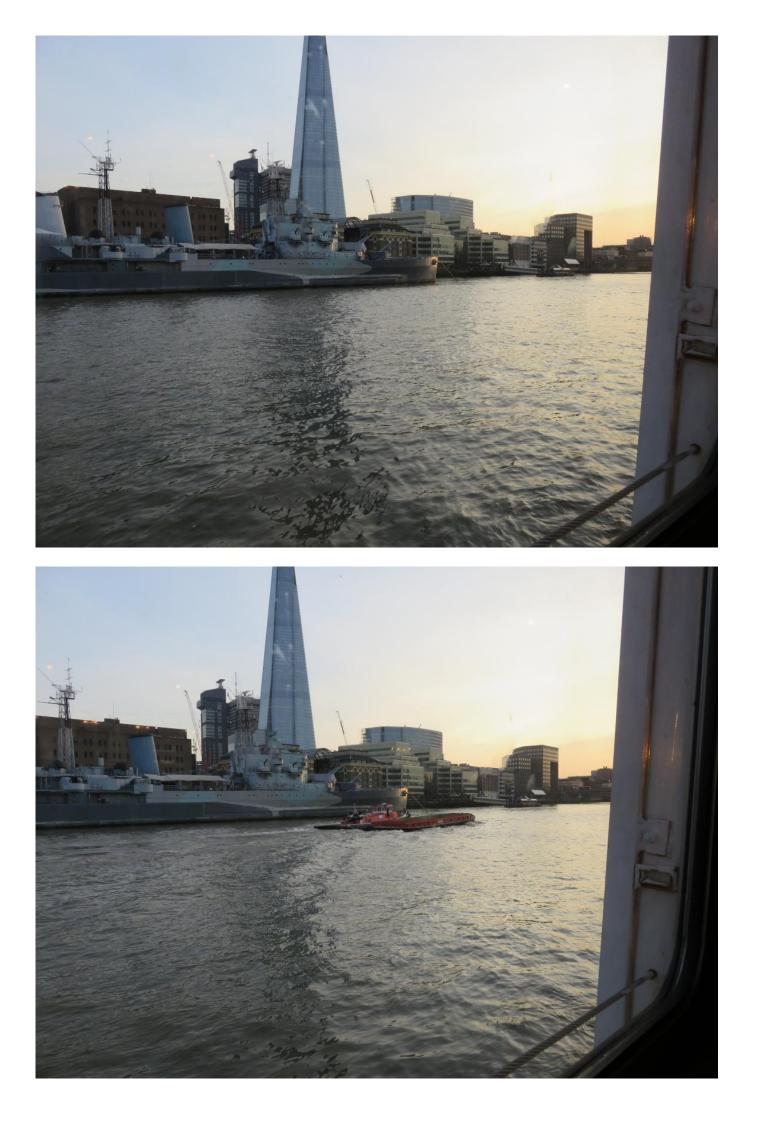
750ms: Finish.

75.0ms: Start displaying contents.



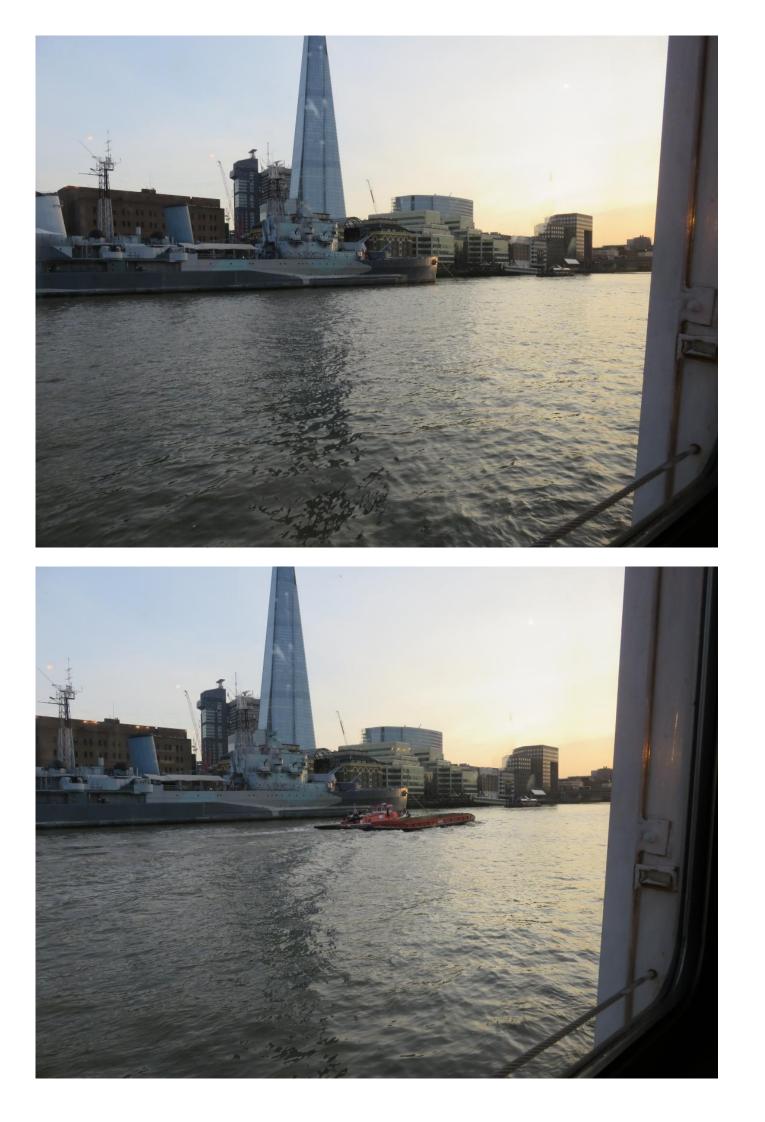
625ms: Finish.

62.5ms: Start displaying contents.



50ms: Start displaying contents.

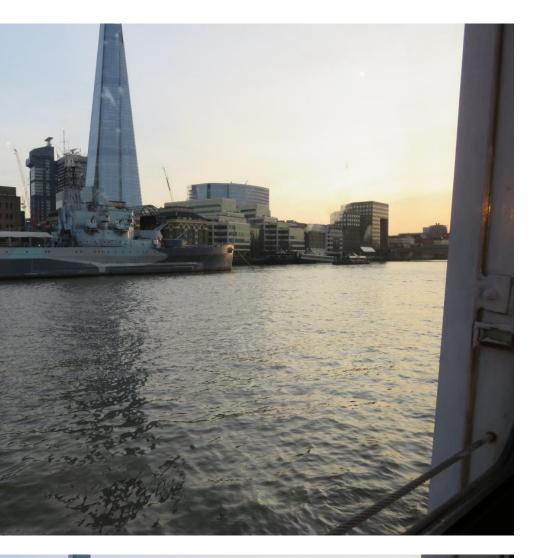
500ms: Finish.



50ms: Start displaying contents.

900ms: Finish.







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900ms: Finish.

Cheaper users pro

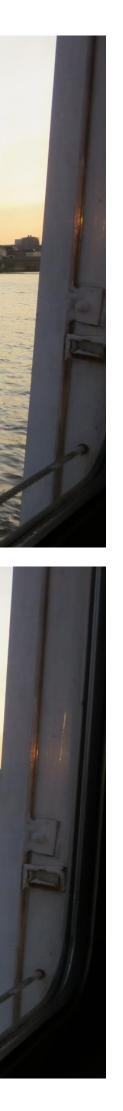




50ms: Start displaying contents.

900ms: Finish.

Cheaper computat users process more



50ms: Start displaying contents.

900ms: Finish.

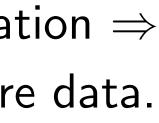
Cheaper computation \Rightarrow users process more data.

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Performance issues disappear for most operations. e.g. open file, clean up.

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"Except, uh, a lot of people have applications whose profiles are mostly flat, because they've spent a lot of time optimizing them." — This view is obsolete. Flat profiles are dying. Already dead for most programs. Larger and larger fraction of code runs freezingly cold, while hot spots run hotter.

Underlying phenomena: Optimization tends to converge. Data volume tends to diverge.

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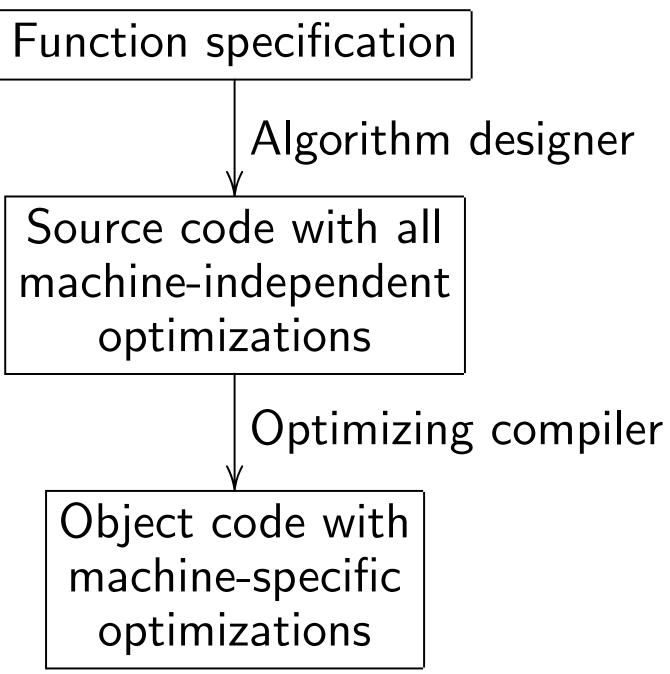
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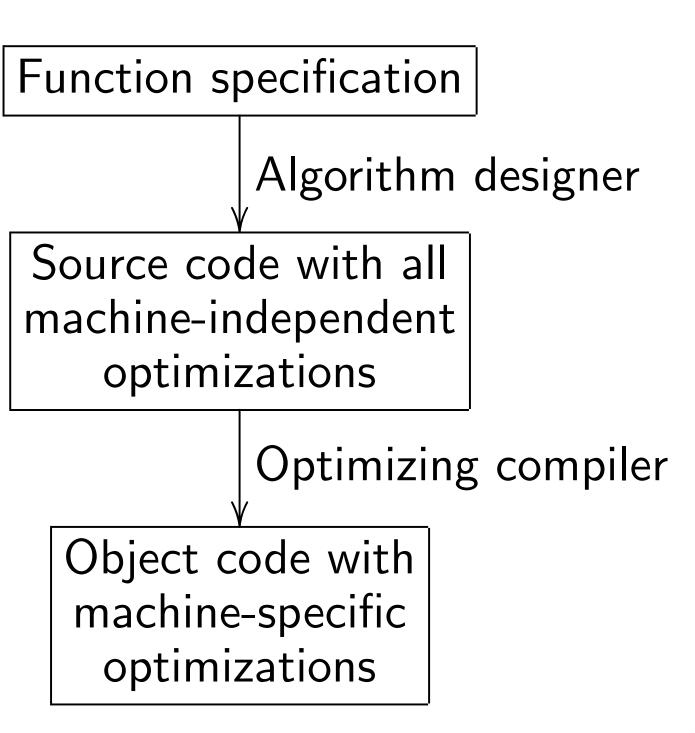
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Algorithm designer

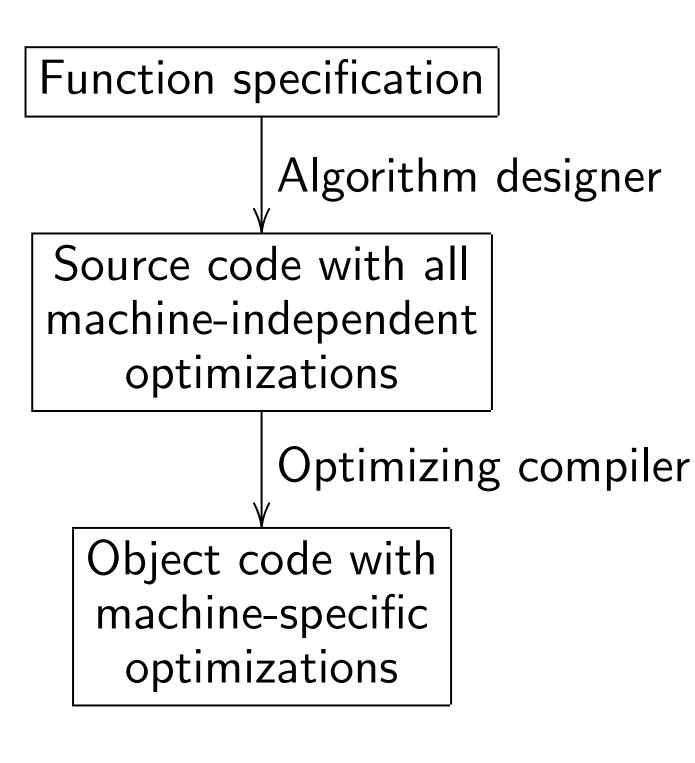
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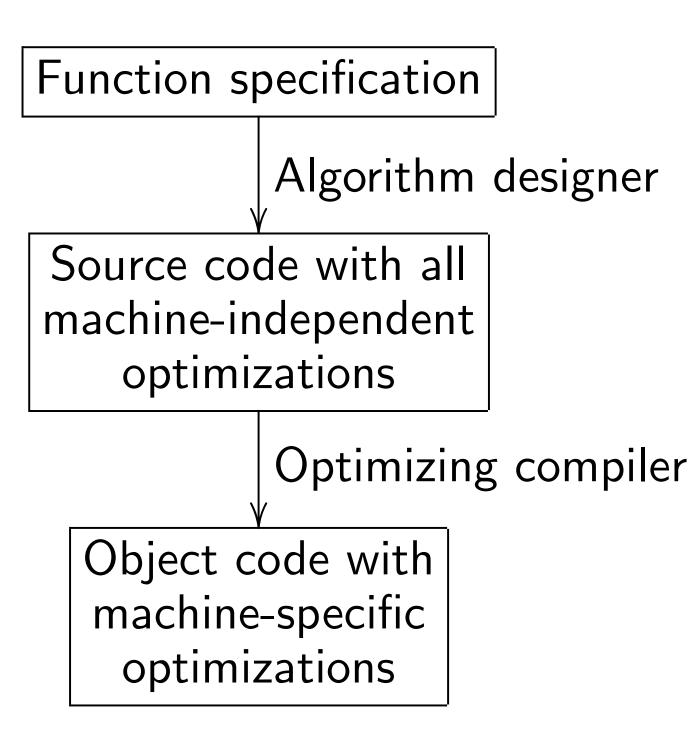
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Minor optimization challenges:

- Pipelining.
- Superscalar processing.

Major optimization challenges:

- Vectorization.
- Many threads; many cores.
- The memory hierarchy; the ring; the mesh.
- Larger-scale parallelism.
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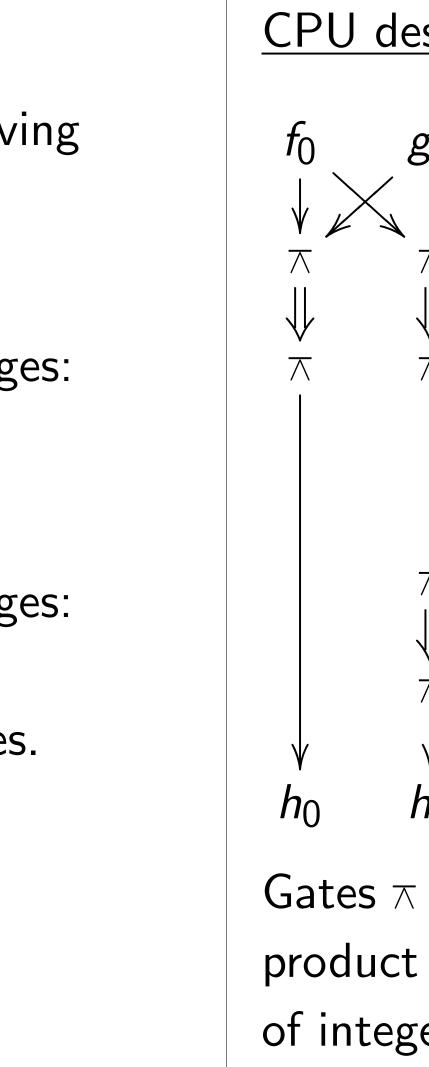
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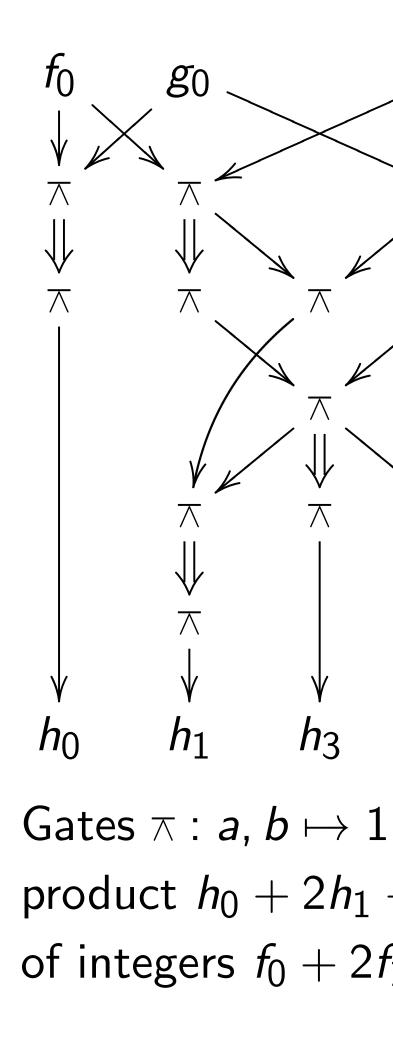
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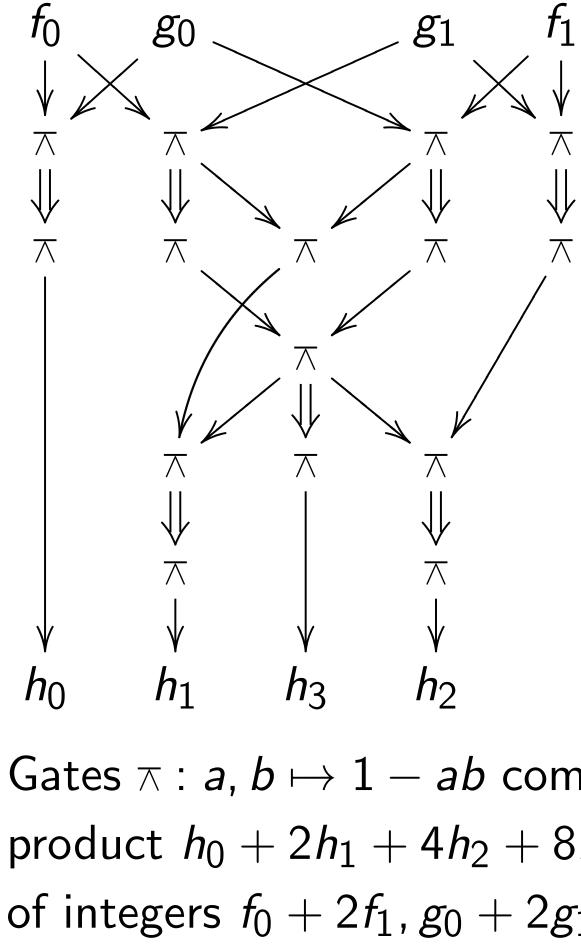
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CPU design in a nutshell



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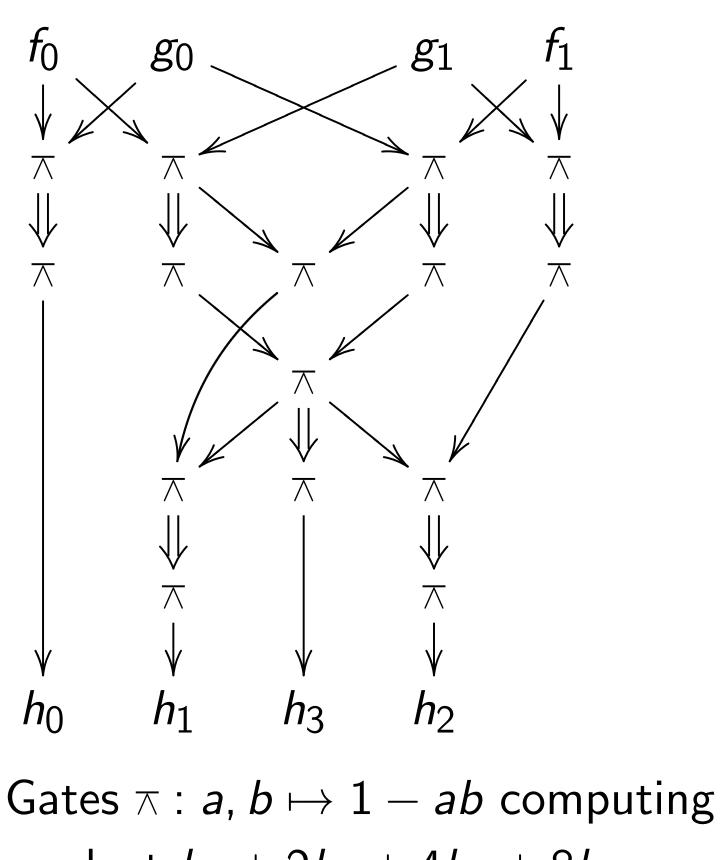
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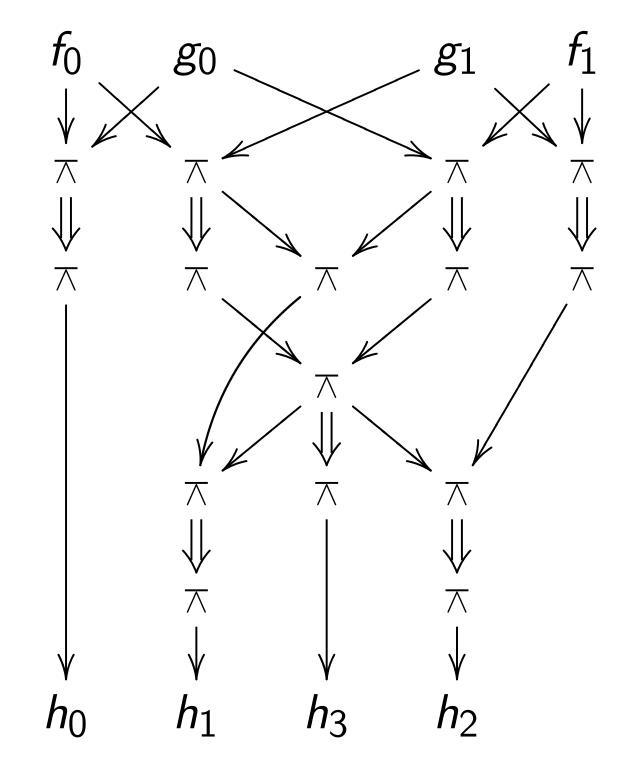
of integers $f_0 + 2f_1$, $g_0 + 2g_1$.

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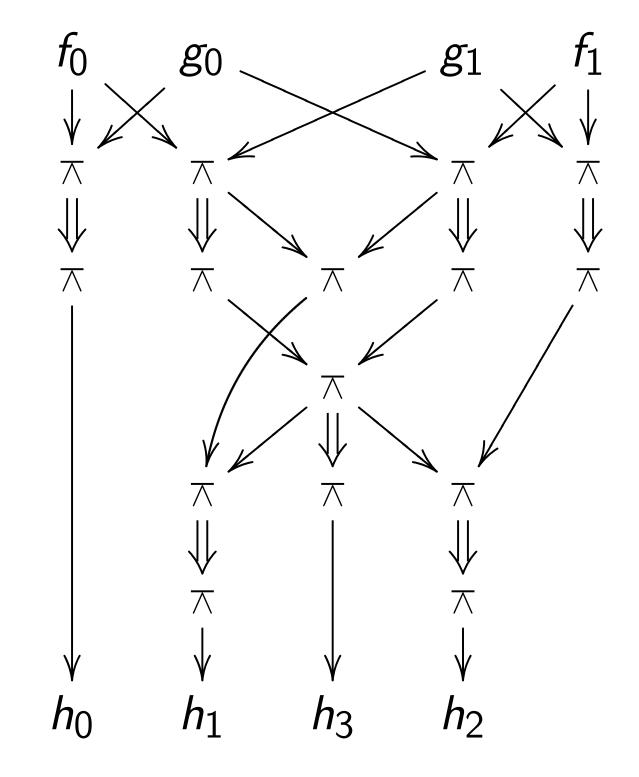
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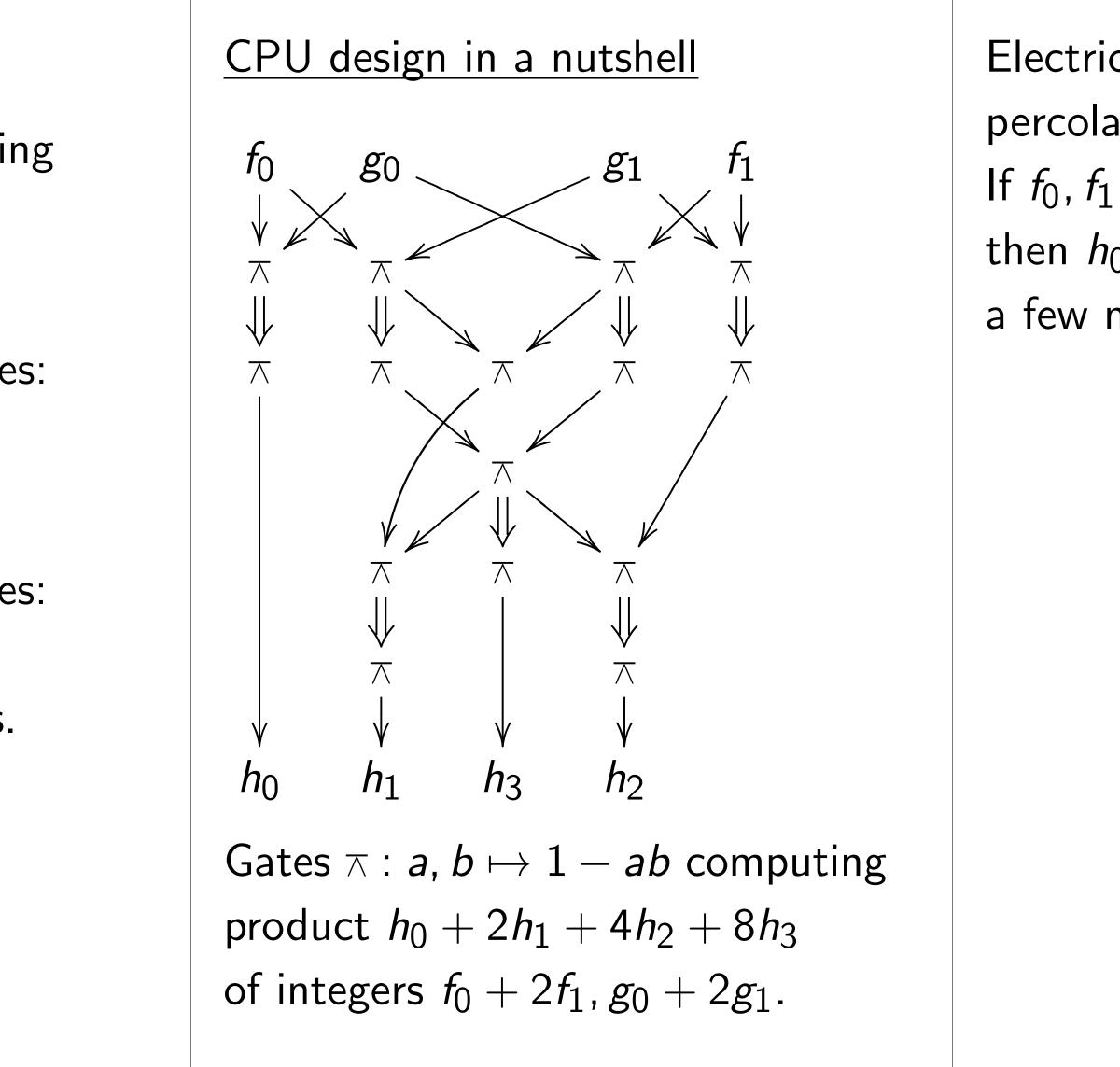
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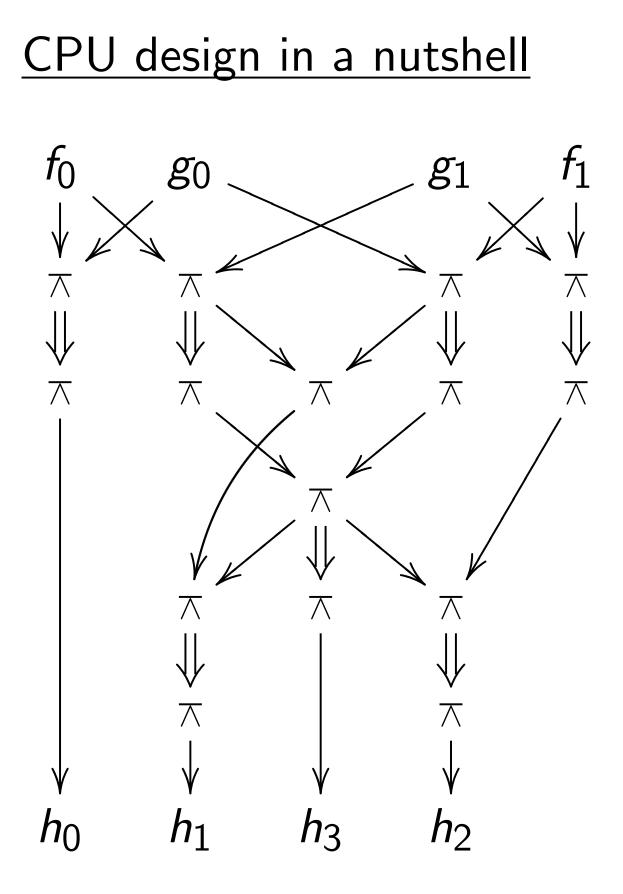
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Electricity takes time to percolate through wires and

If f_0 , f_1 , g_0 , g_1 are stable

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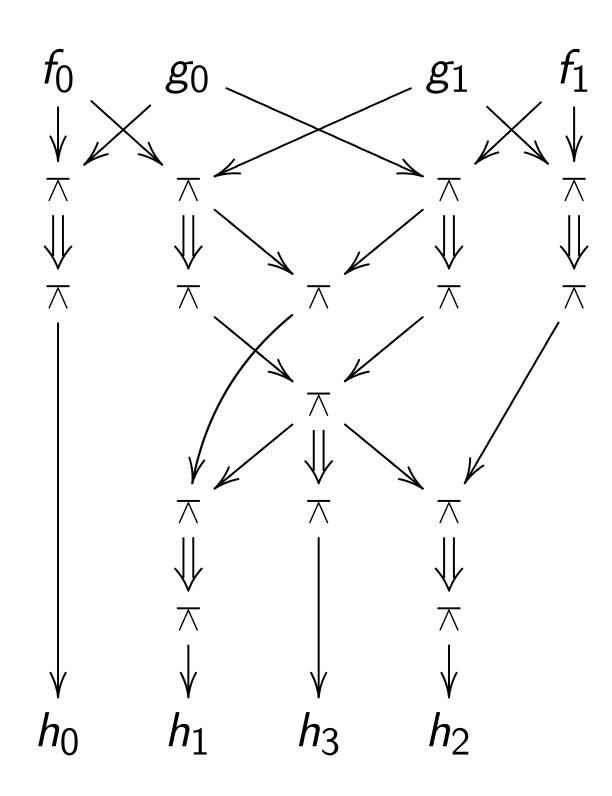


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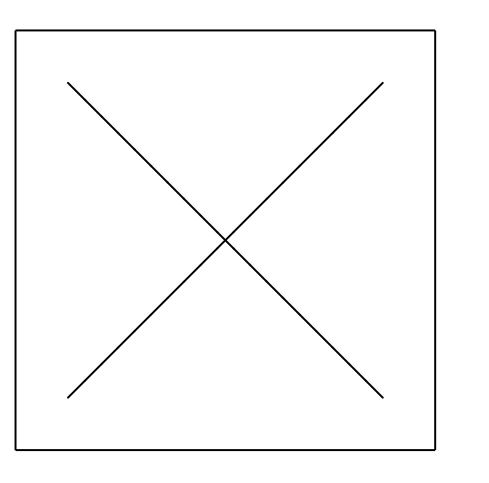
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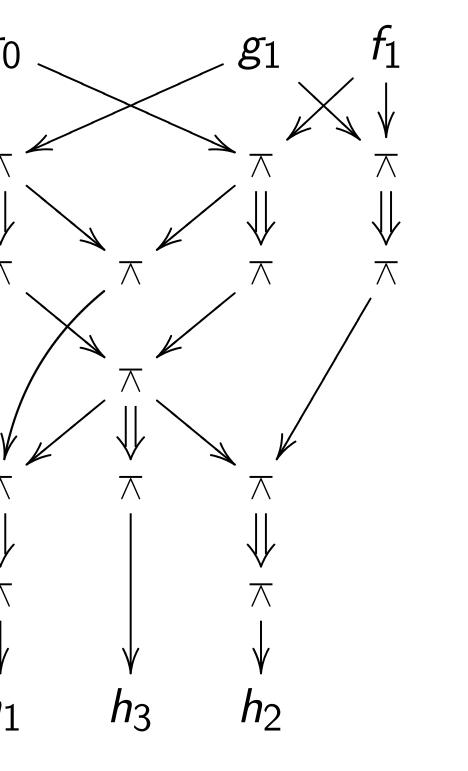
Build circuit with more gates to multiply (e.g.) 32-bit integers:



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- percolate through wires and gates.

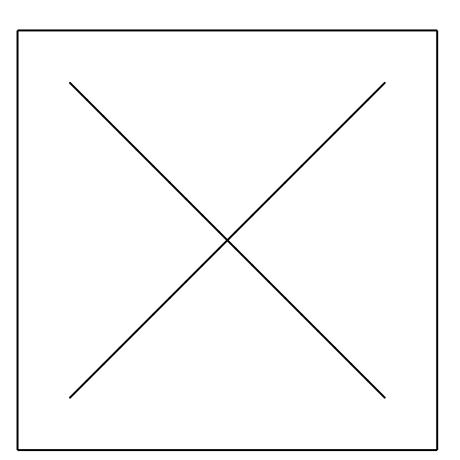
<u>sign in a nutshell</u>



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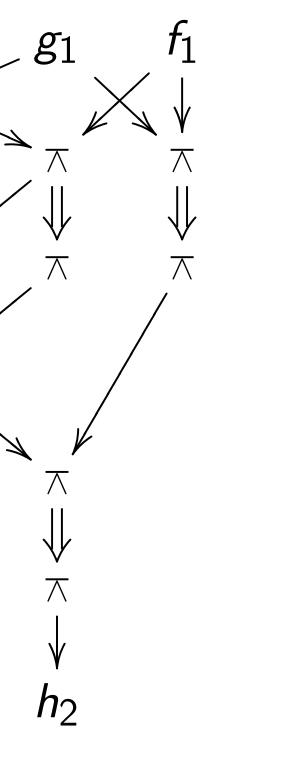


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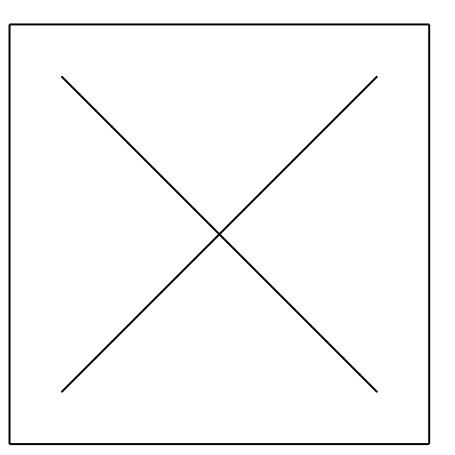


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- ab computing + $4h_2 + 8h_3$ $\frac{1}{1}, g_0 + 2g_1$. Electricity takes time to percolate through wires and gates. If f_0 , f_1 , g_0 , g_1 are stable then h_0 , h_1 , h_2 , h_3 are stable a few moments later.

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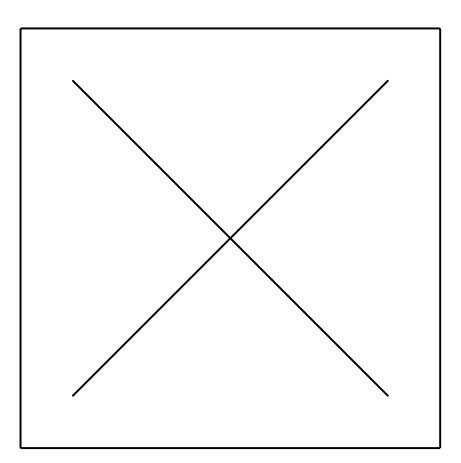


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Build circuit to co 32-bit integer *r_i* given 4-bit integer and 32-bit integers

register read

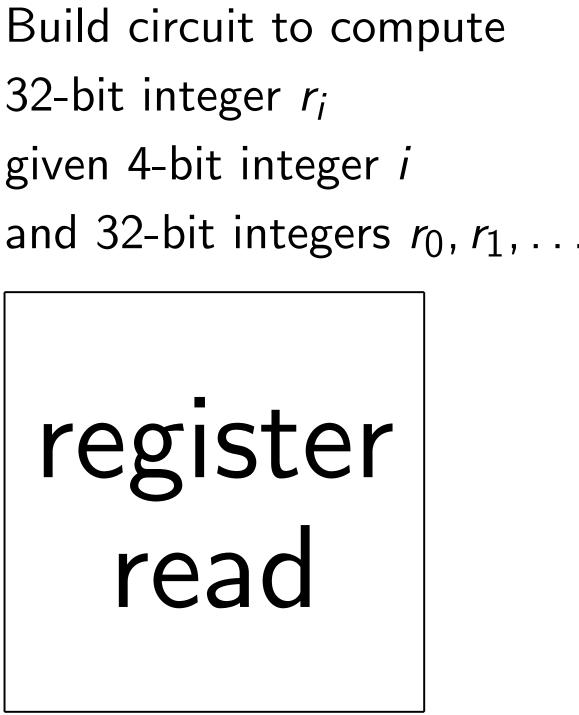
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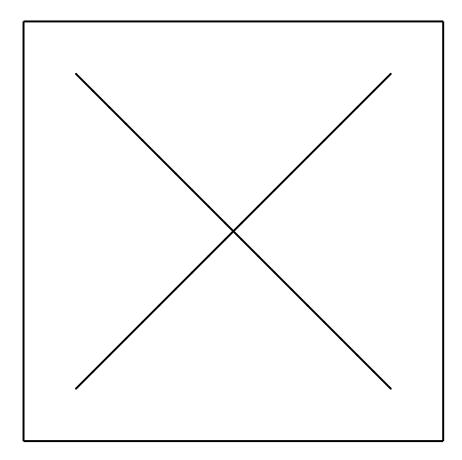
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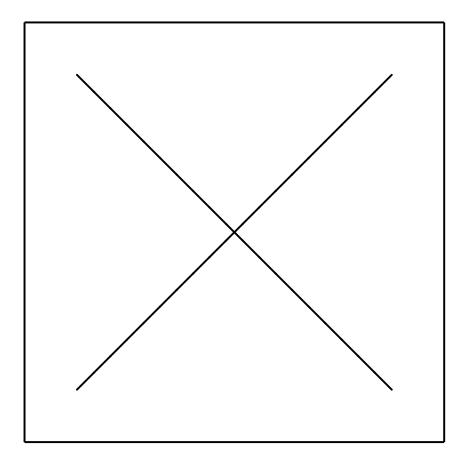


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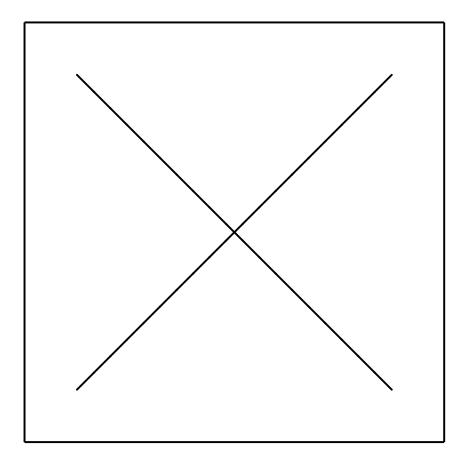
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Build circuit for "register write": $r_0, \ldots, r_{15}, s, i \mapsto r'_0, \ldots, r'_{15}$ where $r'_i = r_j$ except $r'_i = s$.

Build circuit with more gates to multiply (e.g.) 32-bit integers:

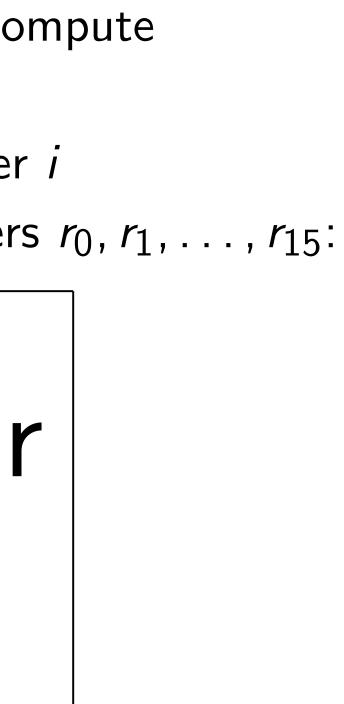


(Details omitted.)

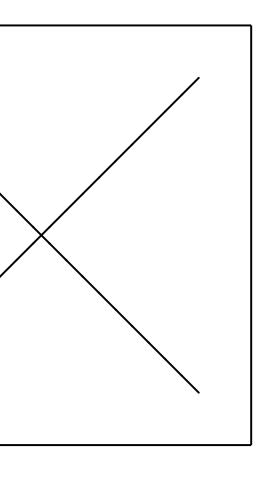
Build circuit to compute 32-bit integer r_i given 4-bit integer i and 32-bit integers $r_0, r_1, ..., r_{15}$:

register read

Build circuit for "register write": $r_0, \ldots, r_{15}, s, i \mapsto r'_0, \ldots, r'_{15}$ where $r'_i = r_j$ except $r'_i = s$. Build circuit for addition. Etc.



- ty takes time to e through wires and gates. g_0, g_1 are stable h_1, h_2, h_3 are stable oments later.
- cuit with more gates ply (e.g.) 32-bit integers:



omitted.)

Build circuit to compute 32-bit integer r_i given 4-bit integer i and 32-bit integers $r_0, r_1, ..., r_{15}$:



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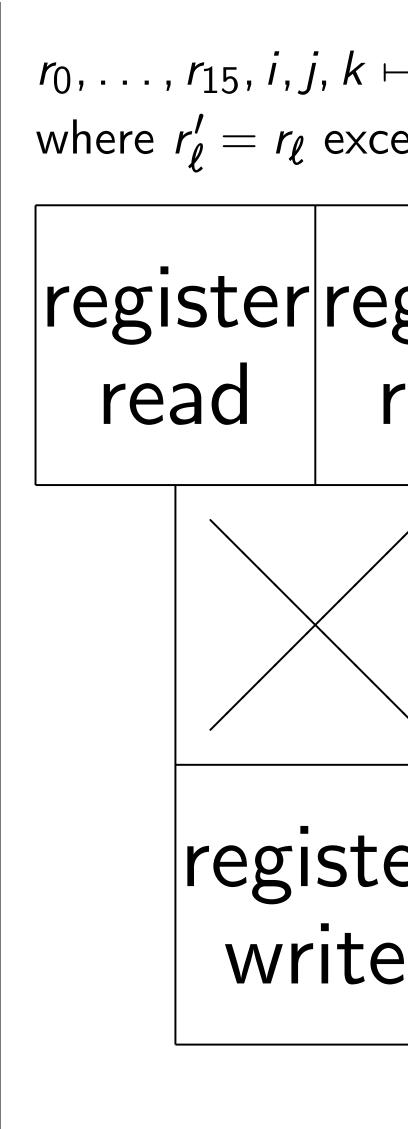
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more gates 32-bit integers: Build circuit to compute 32-bit integer r_i given 4-bit integer *i* and 32-bit integers r_0, r_1, \ldots, r_{15} :

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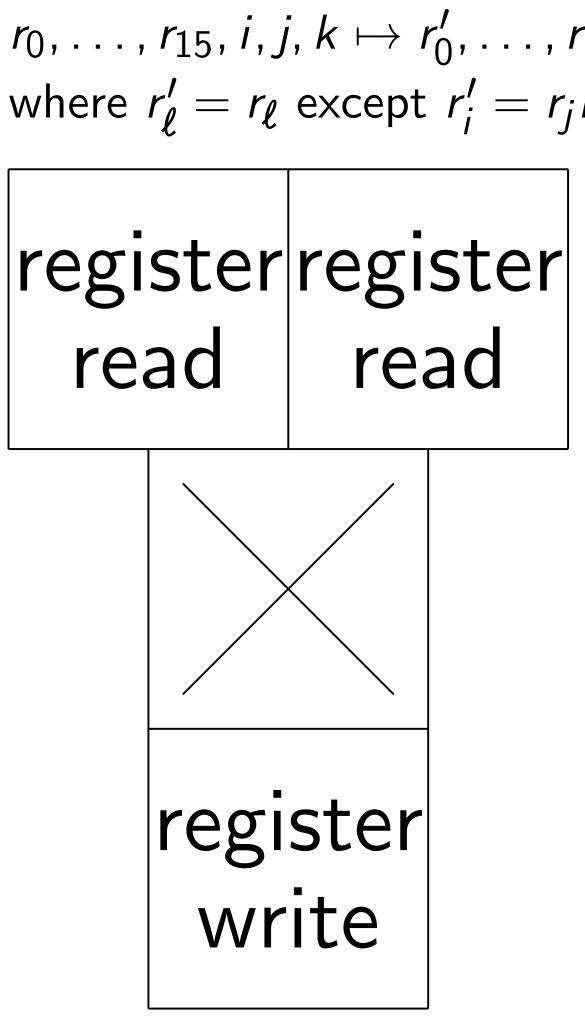
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S gers:



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 $r_0, \ldots, r_{15}, i, j, k \mapsto r'_0, \ldots, r'_{15}$ where $r'_{\ell} = r_{\ell}$ except $r'_i = r_i r_k$: register register read | read register write



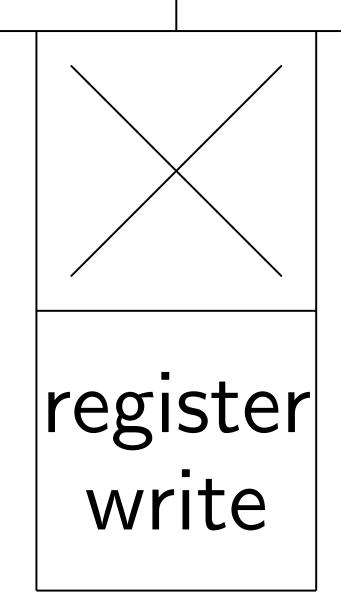
- cuit to compute
- teger r_i
- bit integer i
- oit integers $r_0, r_1, ..., r_{15}$:

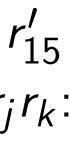
ister ead

cuit for "register write": $r_{15}, s, i \mapsto r'_0, \ldots, r'_{15}$ $= r_i$ except $r'_i = s$. cuit for addition. Etc.

 $r_0, \ldots, r_{15}, i, j, k \mapsto r'_0, \ldots, r'_{15}$ where $r'_{\ell} = r_{\ell}$ except $r'_i = r_i r_k$:

register register read read





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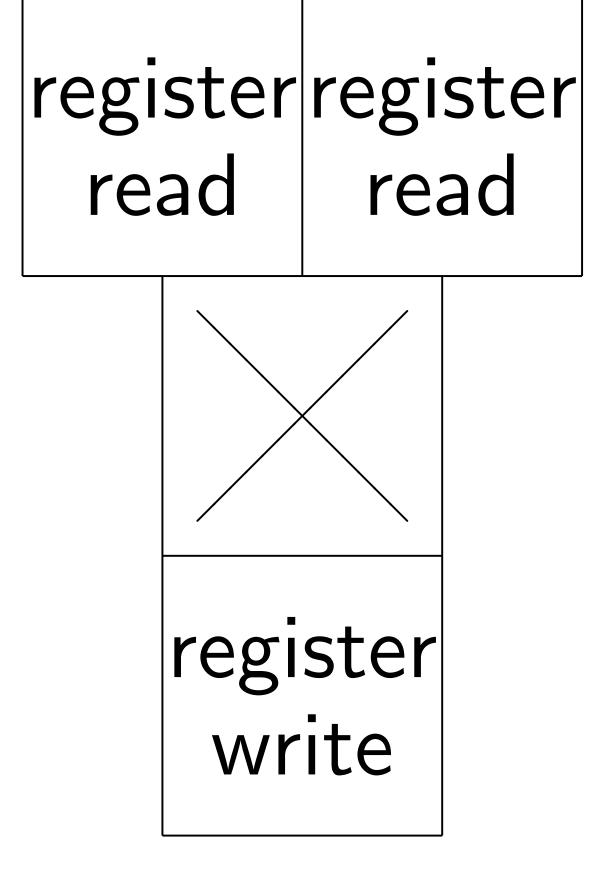
s r_0, r_1, \ldots, r_{15} :

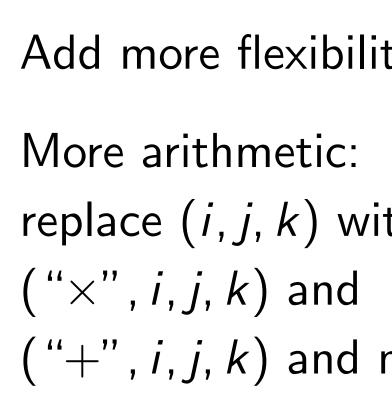
register write": r'_0, \ldots, r'_{15} pt $r'_i = s$.

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$$r_0, \ldots, r_{15}, i, j, k \mapsto r'_0, \ldots, r'_{15}$$

where $r'_{\ell} = r_{\ell}$ except $r'_i = r_j r_k$:





$$r_{0}, \ldots, r_{15}, i, j, k \mapsto r_{0}^{\prime}, \ldots, r_{15}^{\prime}$$

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arithmetic:

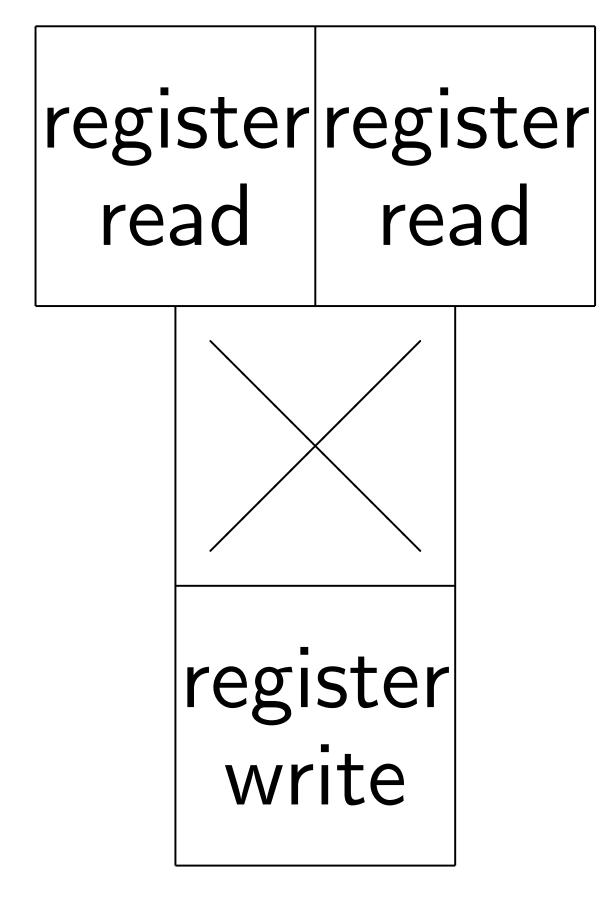
e(i, j, k) with

i, *j*, *k*) and

i, j, k) and more optio

$$r_0, \ldots, r_{15}, i, j, k \mapsto r'_0, \ldots, r'_{15}$$

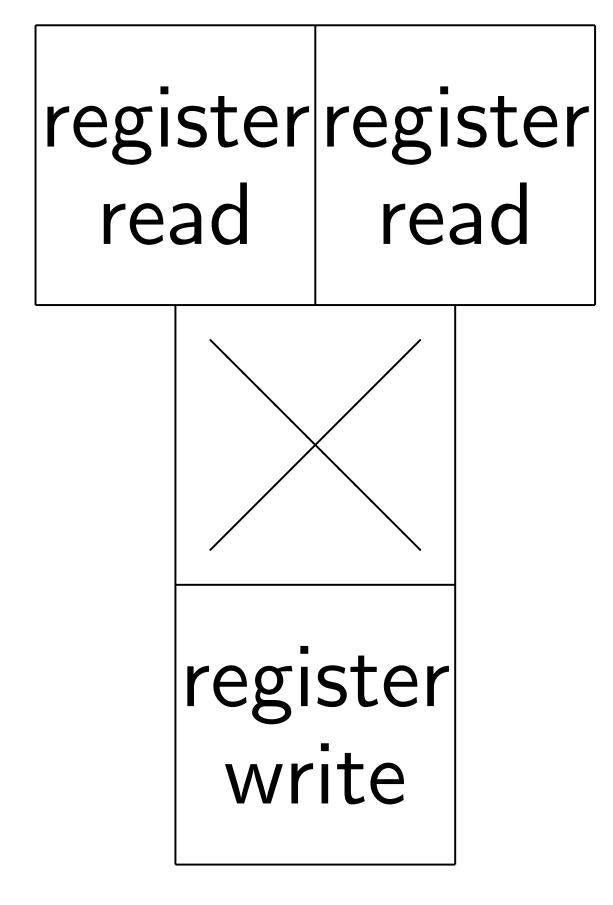
where $r'_{\ell} = r_{\ell}$ except $r'_i = r_j r_k$:



More arithmetic: replace (i, j, k) with $(``\times'', i, j, k)$ and ("+", i, j, k) and more options.

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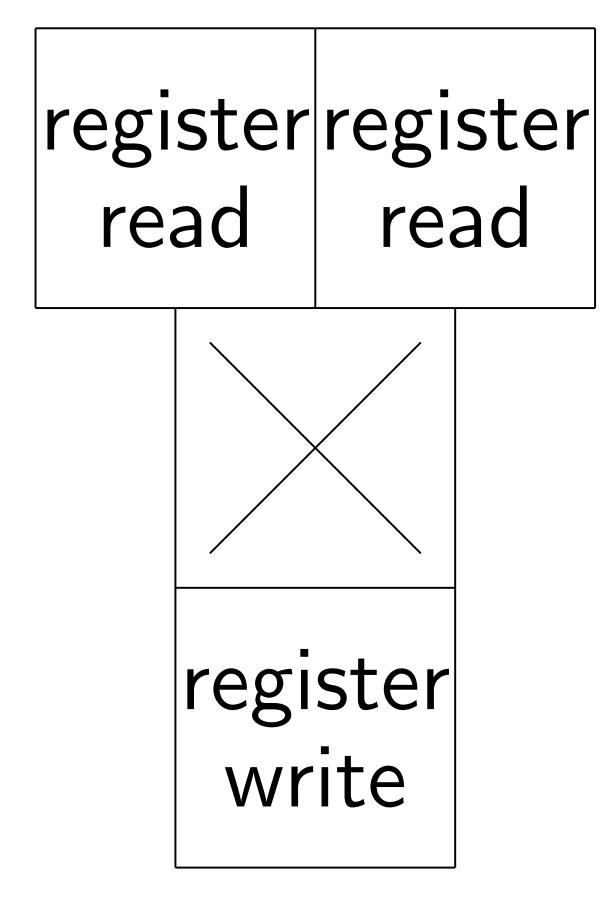


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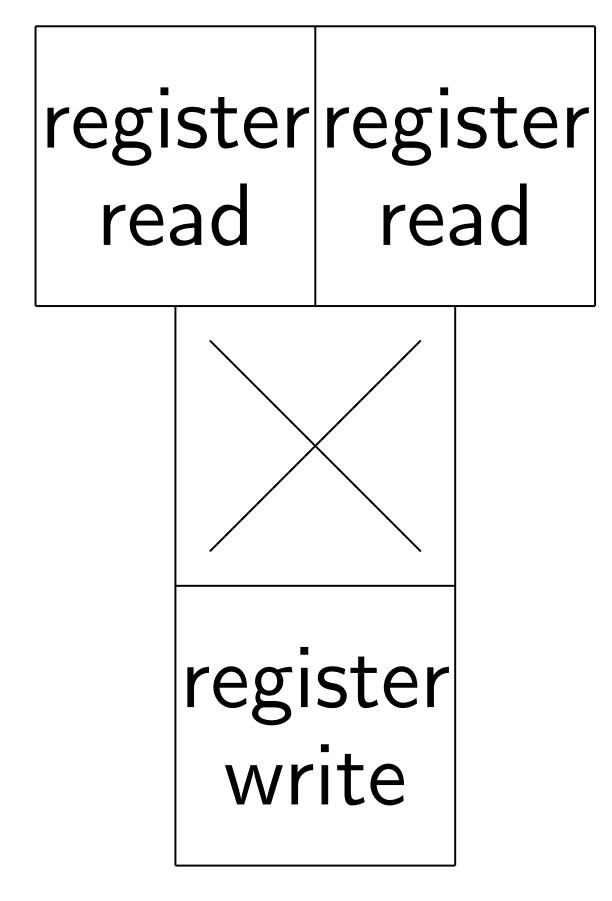
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More (but slower) storage: "load" from and "store" to larger "RAM" arrays.

$$r_{15}, i, j, k \mapsto r'_0, \dots, r'_{15}$$

= r_ℓ except $r'_i = r_j r_k$:

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Add more flexibility.

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/ 15 r_k :

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- Hook $(p, r_0, ..., r_{15})$
- flip-flops into circuit inputs.
- Hook outputs $(p', r'_0, \ldots, r'_{1^{r}})$ into the same flip-flops.
- At each "clock tick",
- flip-flops are overwritten
- with the outputs.

Clock needs to be slow enou for electricity to percolate all the way through the circ from flip-flops to flip-flops.

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Clock needs to be slow enough for electricity to percolate all the way through the circuit, from flip-flops to flip-flops. re flexibility.

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- *j*, *k*) and
- j, k) and more options.
- tion fetch":
- i_p, j_p, k_p, p' .
- tion decode": ression of compressed or o_p, i_p, j_p, k_p, p' .
- ut slower) storage: rom and "store" to RAM" arrays.

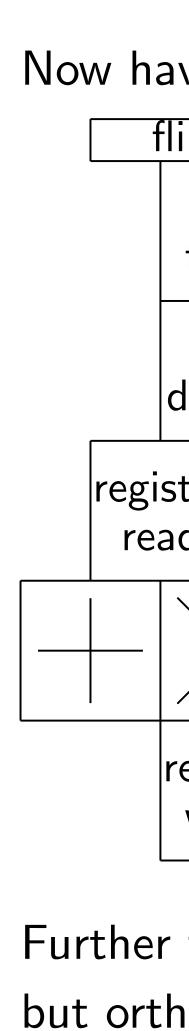
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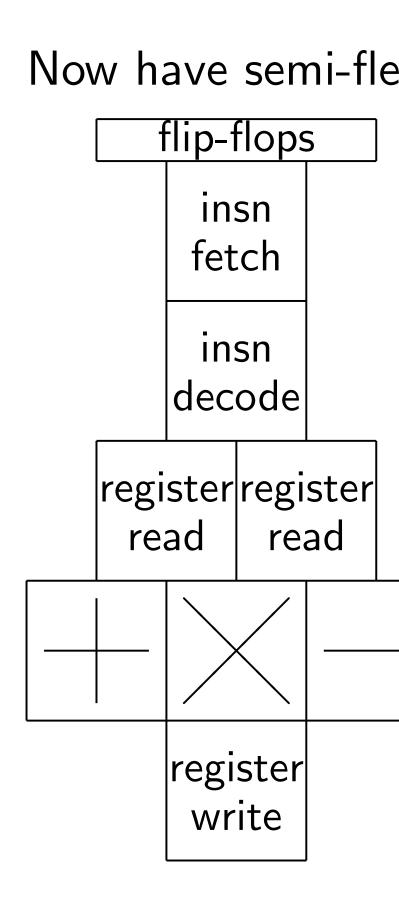
compressed $_{p}, k_{p}, p'$.

storage: 'store'' to

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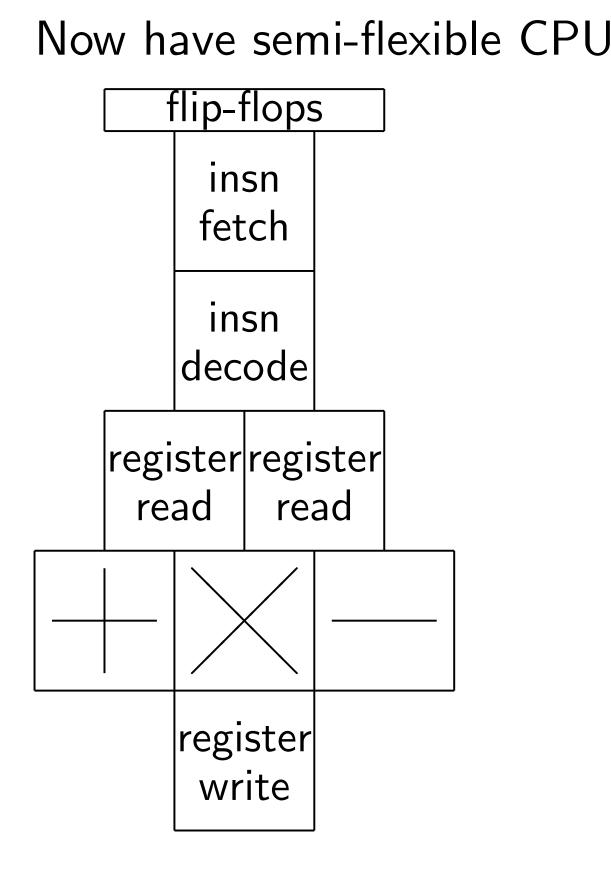
Further flexibility i but orthogonal to

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Clock needs to be slow enough for electricity to percolate all the way through the circuit, from flip-flops to flip-flops.



Further flexibility is useful but orthogonal to this talk.

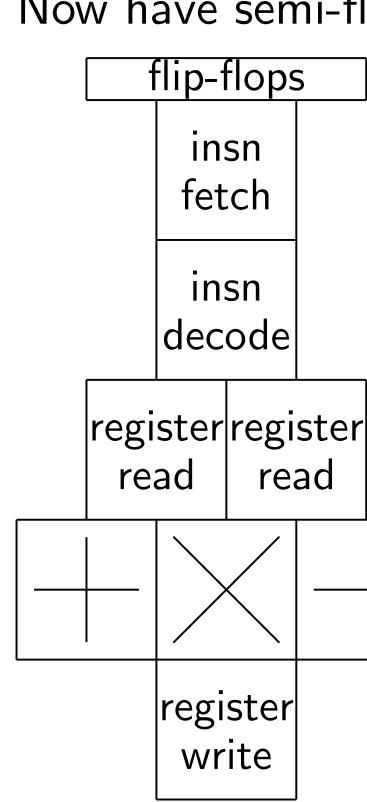
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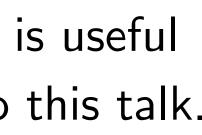
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Clock needs to be slow enough for electricity to percolate all the way through the circuit, from flip-flops to flip-flops.



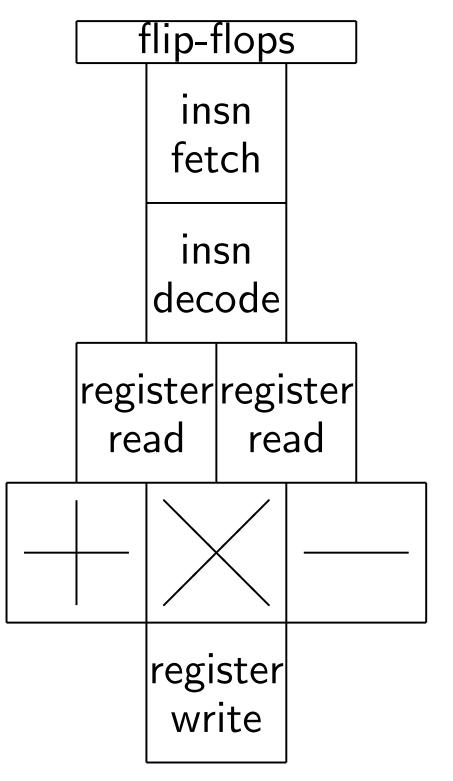
Further flexibility is useful but orthogonal to this talk.

Now have semi-flexible CPU:



- lip-flops"
- $(p, r_0, \ldots, r_{15}).$
- (r_0, \ldots, r_{15})
- s into circuit inputs.
- tputs $(p', r'_0, \ldots, r'_{15})$ same flip-flops.
- "clock tick",
- are overwritten
- outputs.
- eeds to be slow enough ricity to percolate any through the circuit, oflops to flip-flops.

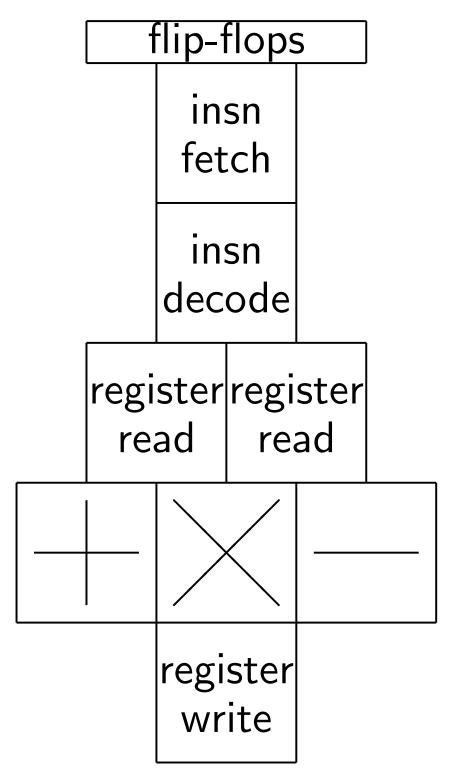
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$$r'_0, \ldots, r'_{15}$$
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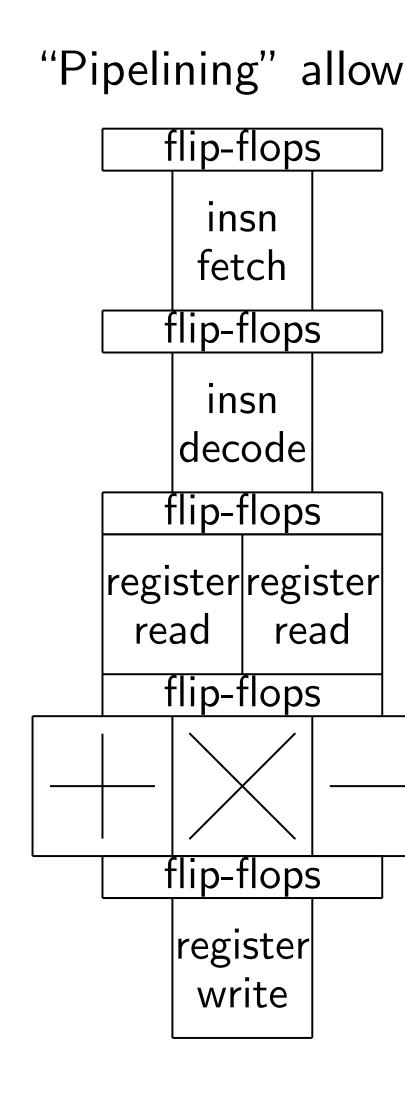
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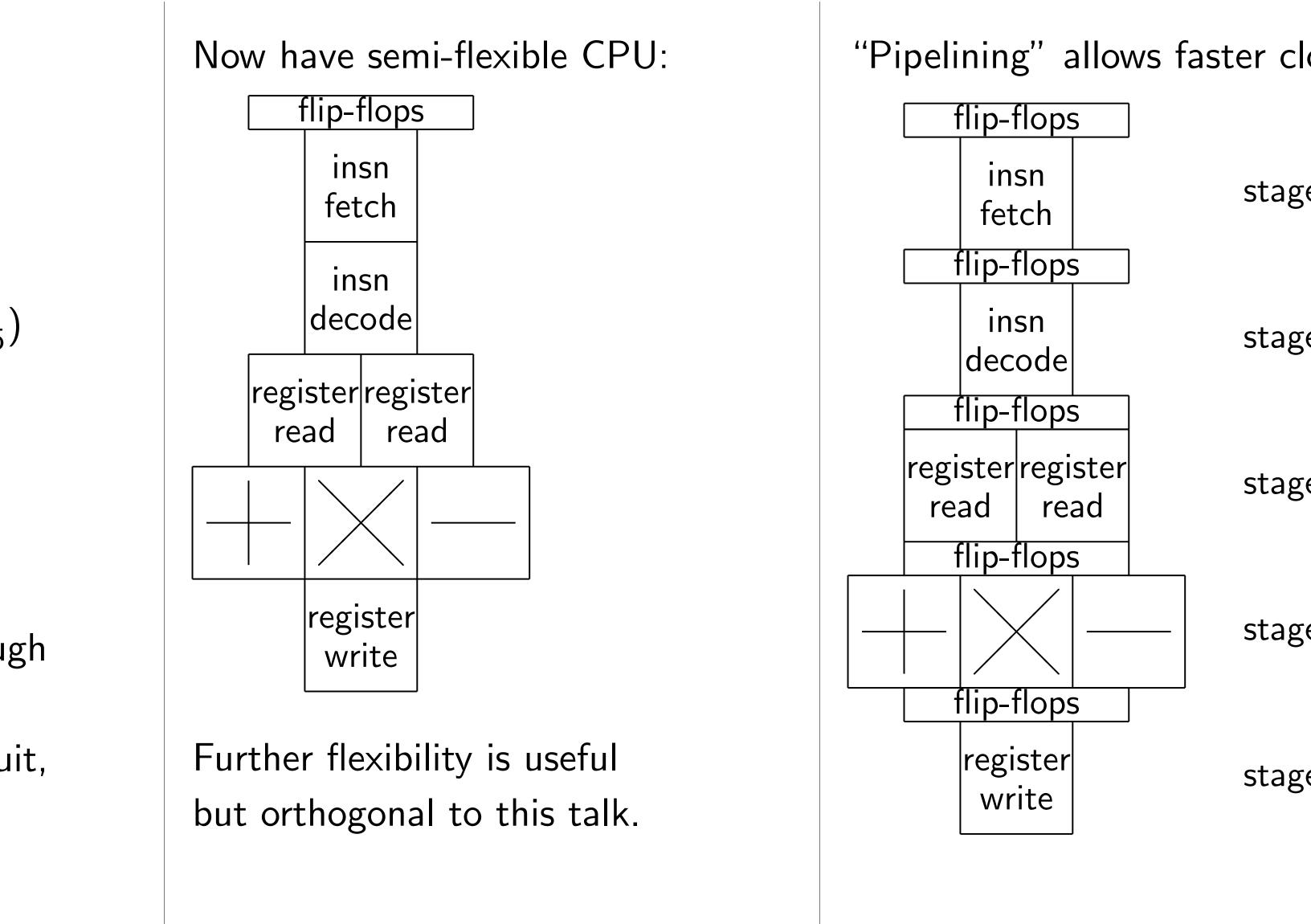
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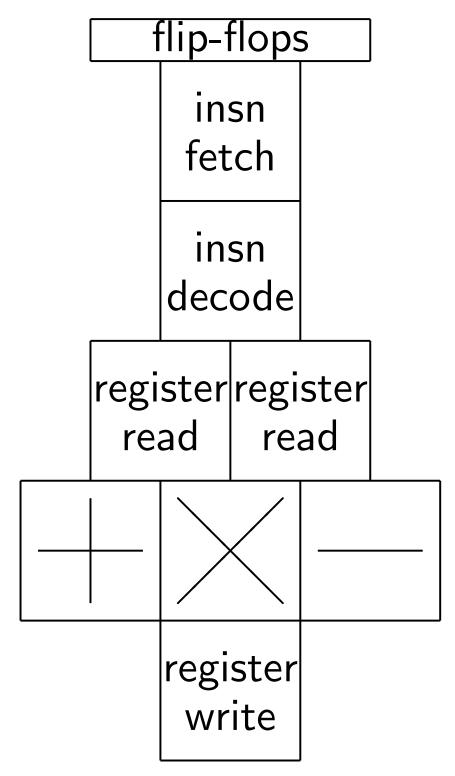
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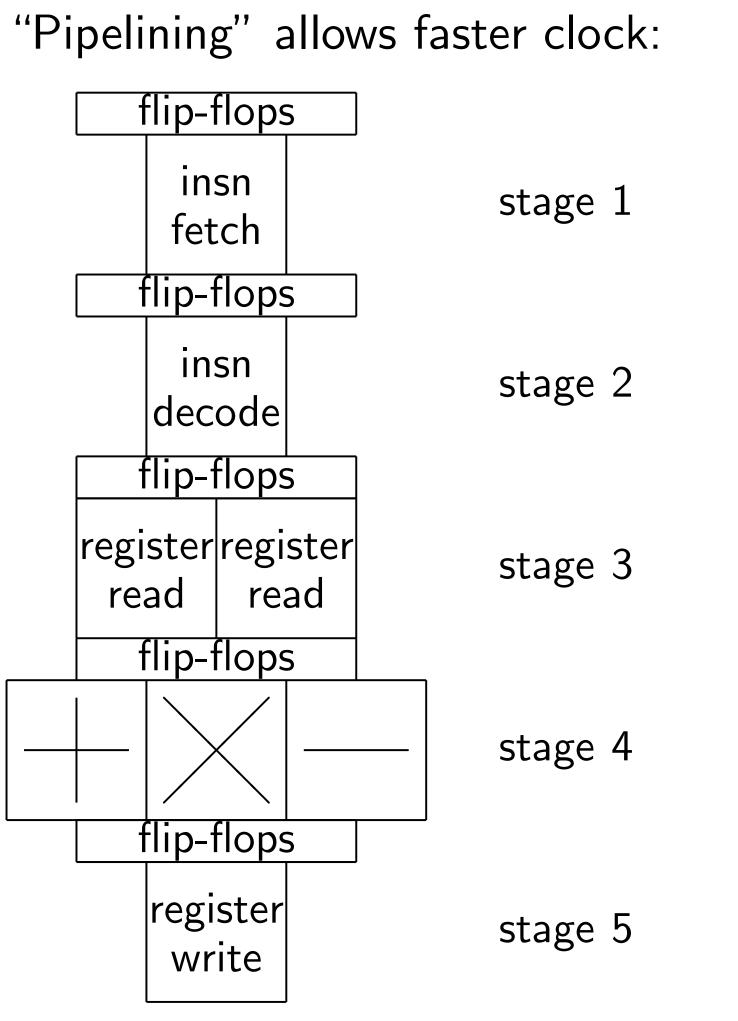


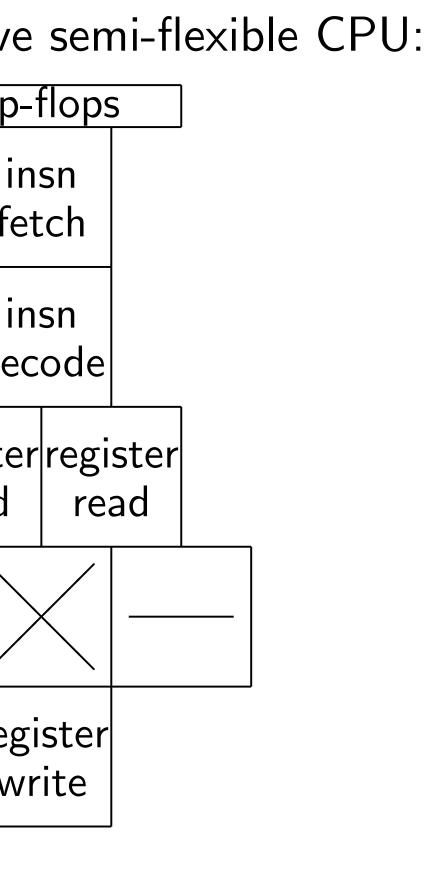






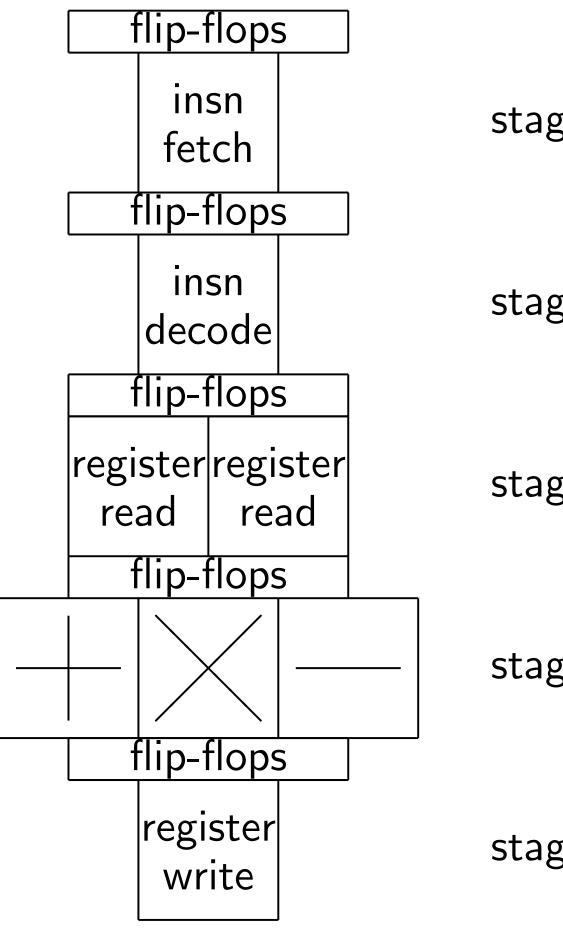
Further flexibility is useful but orthogonal to this talk.





flexibility is useful ogonal to this talk.

"Pipelining" allows faster clock:



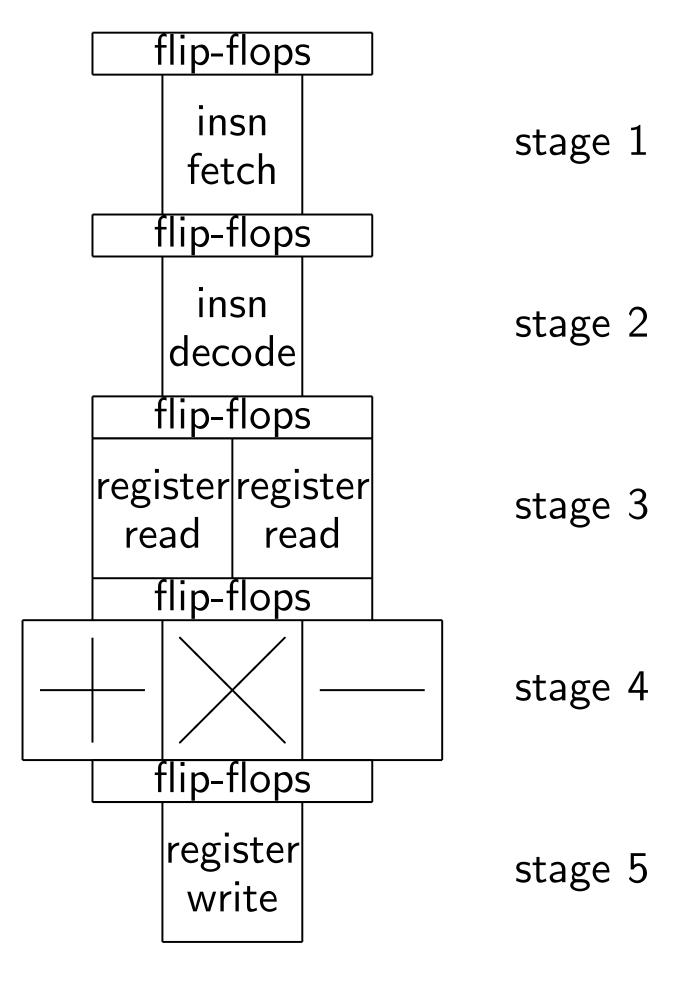
stage 1 stage 2 stage 3 stage 4 stage 5

Goal: St one tick Instructi reads ne feeds p'After ne instructi uncomp while ins reads an Some ex Also ext

- preserve
- e.g., sta



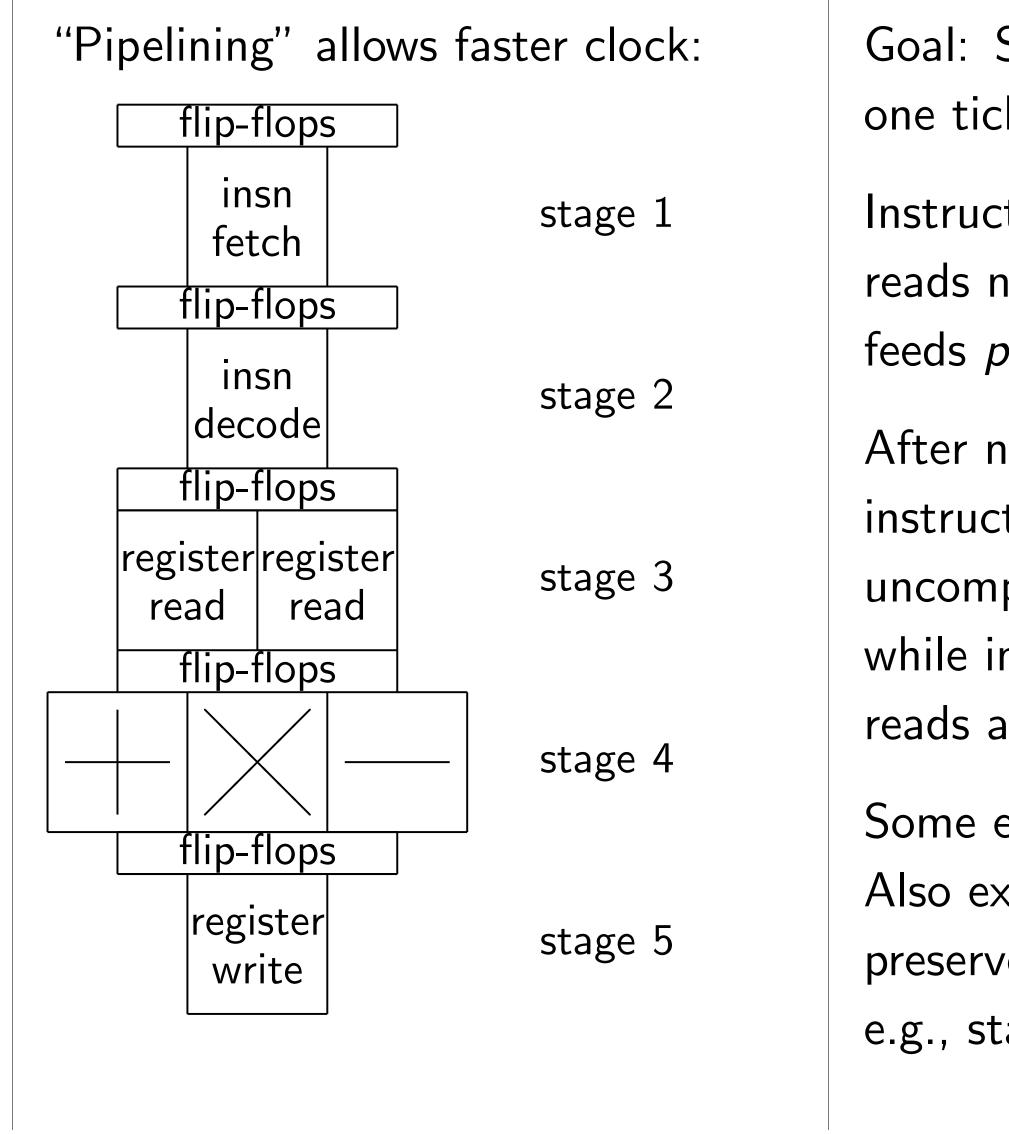
"Pipelining" allows faster clock:



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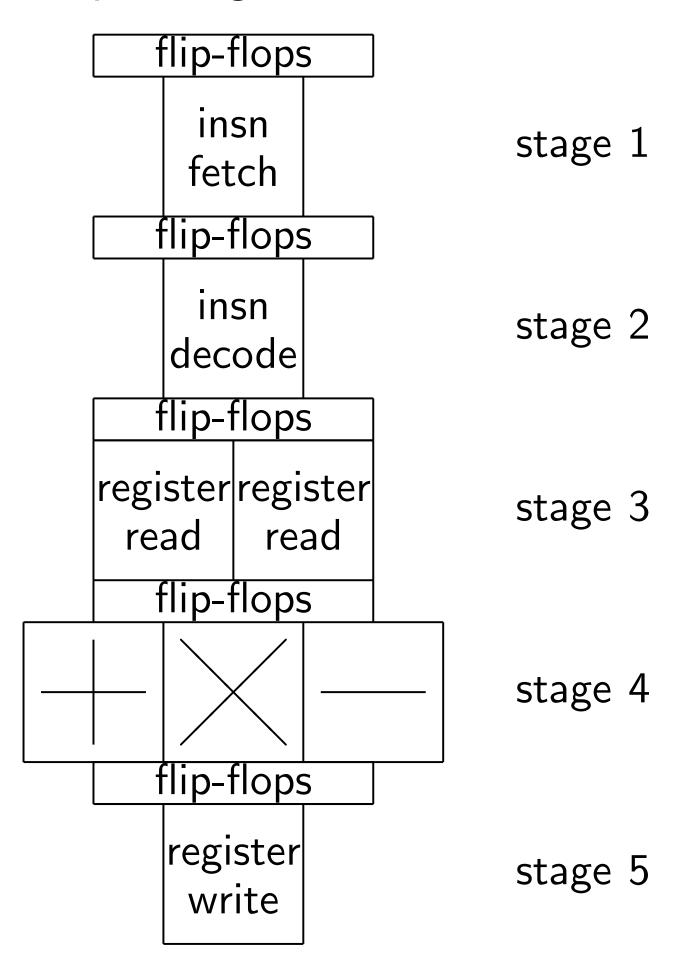
Goal: Stage *n* har one tick after stag Instruction fetch reads next instruct feeds p' back, sen After next clock ti instruction decode uncompresses this while instruction f reads another inst Some extra flip-flc Also extra area to preserve instructio e.g., stall on read-



Goal: Stage n handles instruon one tick after stage n - 1.

- Instruction fetch
- reads next instruction,
- feeds p' back, sends instruct
- After next clock tick,
- instruction decode
- uncompresses this instructio
- while instruction fetch
- reads another instruction.
- Some extra flip-flop area.
- Also extra area to
- preserve instruction semantic
- e.g., stall on read-after-write

"Pipelining" allows faster clock:



Goal: Stage *n* handles instruction one tick after stage n-1. Instruction fetch reads next instruction, feeds p' back, sends instruction. After next clock tick, instruction decode uncompresses this instruction, while instruction fetch reads another instruction. Some extra flip-flop area. Also extra area to preserve instruction semantics: e.g., stall on read-after-write.

ing" allows p-flops	s faster clock:	Goal: Stage n handles instron one tick after stage $n - 1$.
insn fetch	stage 1	Instruction fetch
p-flops insn	stage 2	reads next instruction, feeds <i>p</i> ′ back, sends instruc
ecode p-flops	U	After next clock tick, instruction decode
er register I read	stage 3	uncompresses this instruction
p-flops	– stage 4	while instruction fetch reads another instruction.
p-flops		Some extra flip-flop area. Also extra area to
egister write	stage 5	preserve instruction semant e.g., stall on read-after-writ

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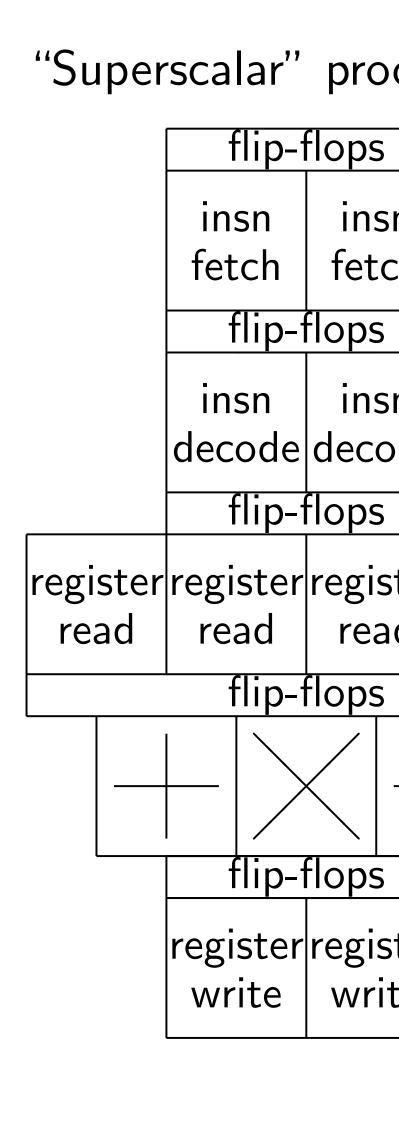
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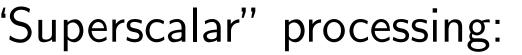


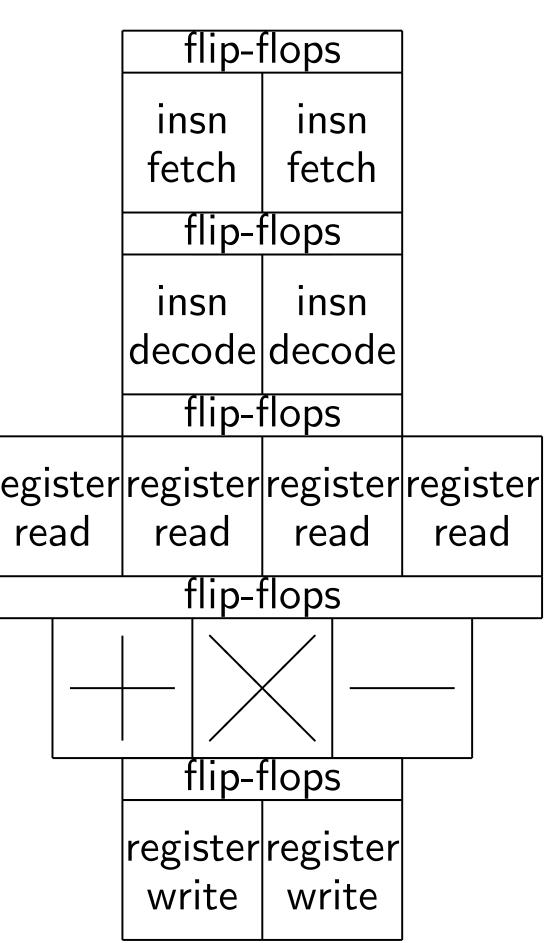
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s faster clock:	Goal: Stage <i>n</i> handles instruction one tick after stage $n - 1$.
stage 1	Instruction fetch reads next instruction,
stage 2	feeds p' back, sends instruction.
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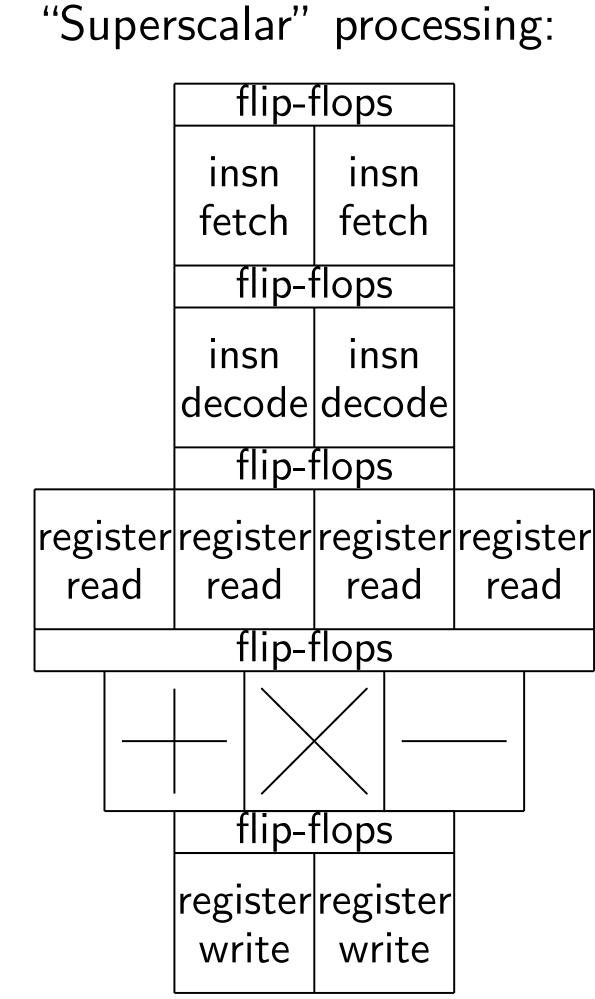
read

Goal: Stage *n* handles instruction one tick after stage n-1.

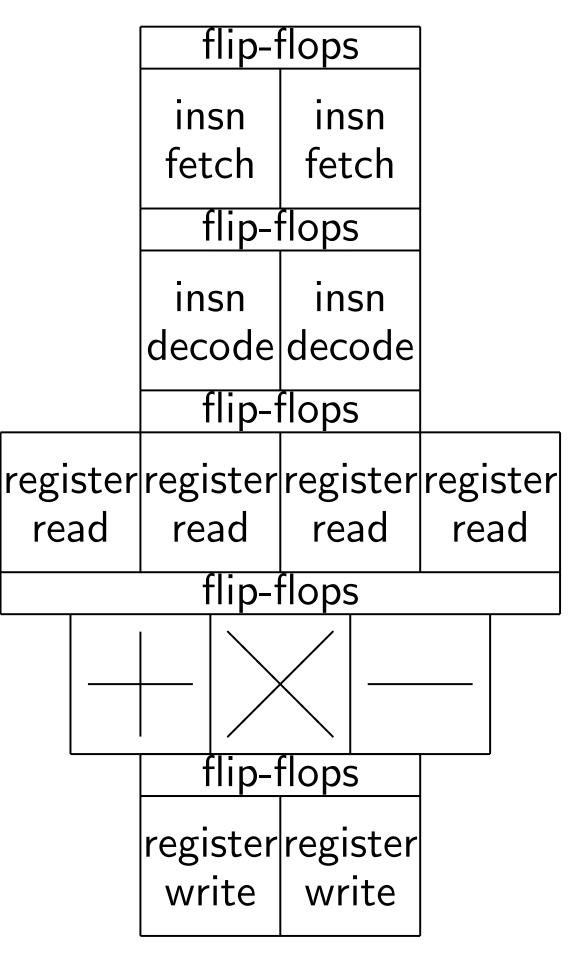
Instruction fetch reads next instruction, feeds p' back, sends instruction.

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- tage n handles instruction after stage n 1.
- on fetch
- xt instruction,
- back, sends instruction.
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Expand into *n*-ve ARM "N Intel "A Intel "A GPUs ha dles instruction n = 1.

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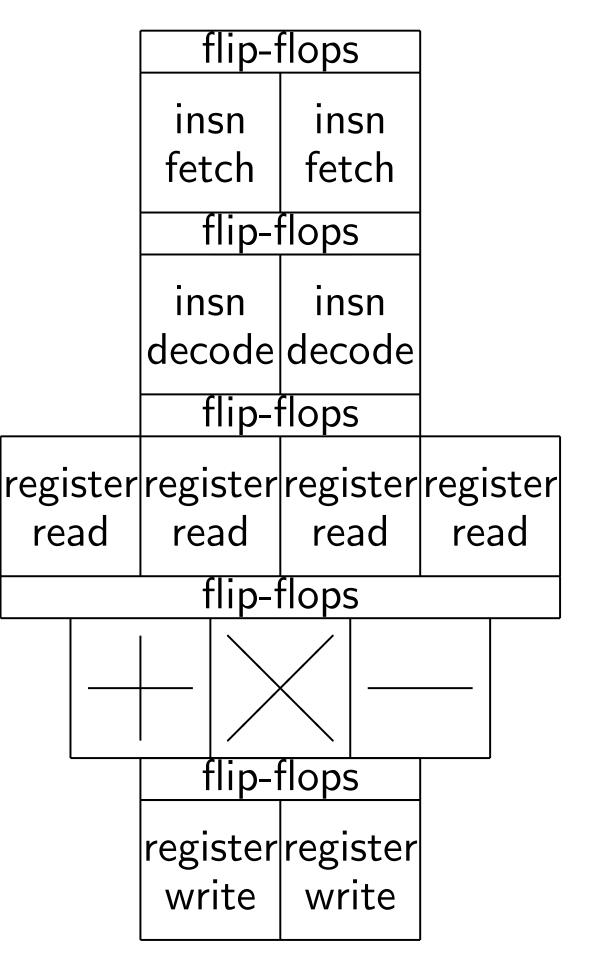
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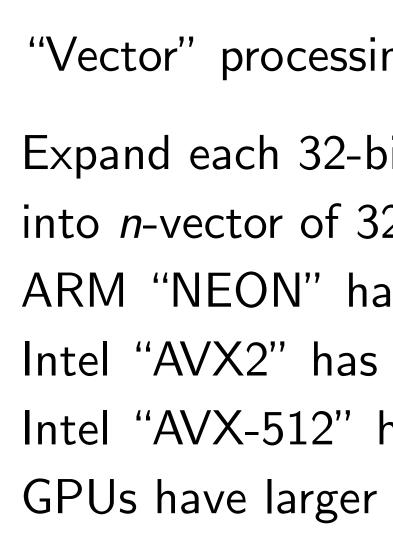
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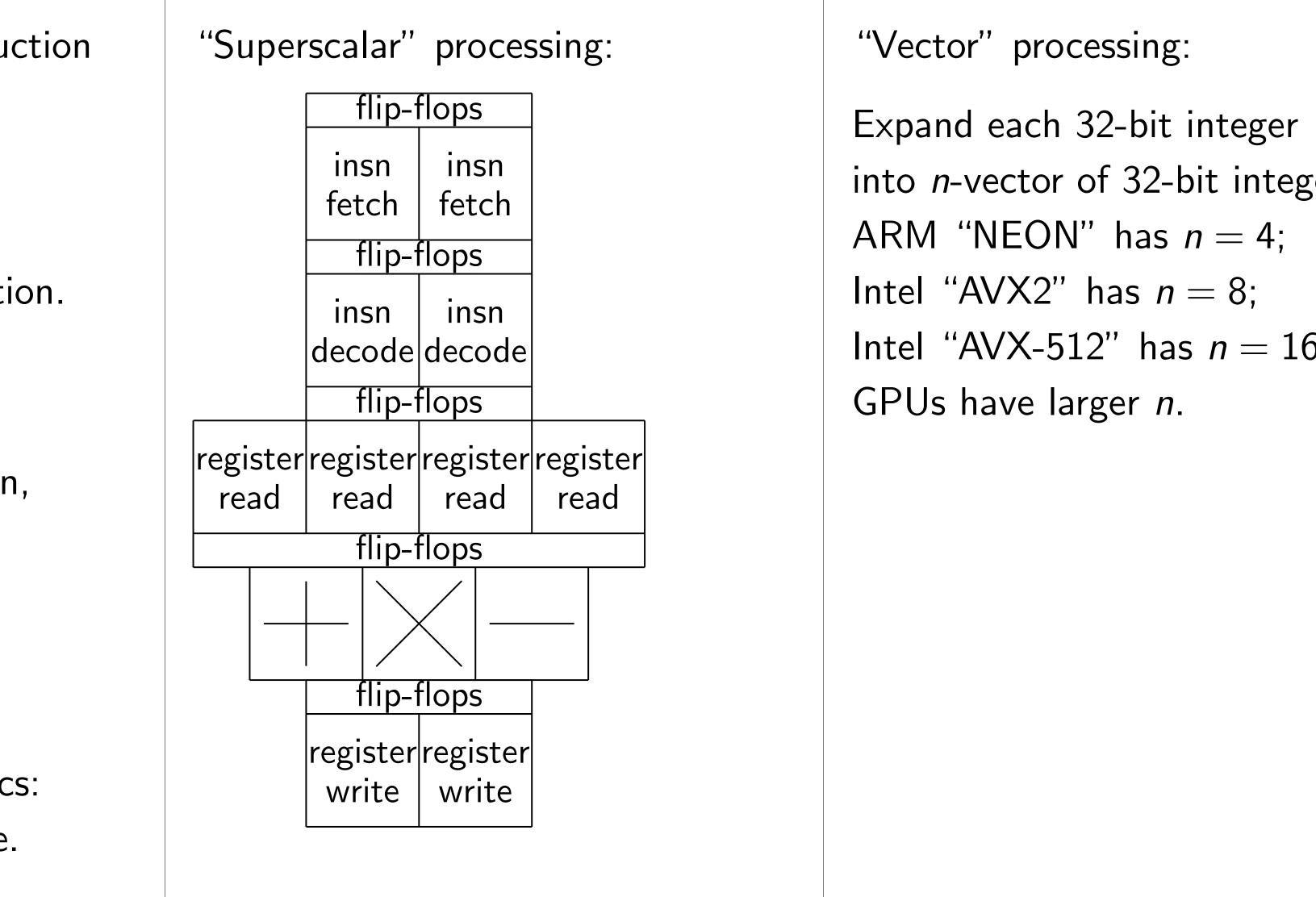
ruction.

p area.

n semantics: after-write. "Superscalar" processing:







into *n*-vector of 32-bit integ

	flip-1		
	insn fetch	insn fetch	
	flip-flops		
	insn decode	insn decode	
	flip-1	flops	
register read	register read	register read	register read
	flip-1	flops	
		$\langle -$	
	flip-1	flops	
		register write	

"Vector" processing:

Expand each 32-bit integer into *n*-vector of 32-bit integers. ARM "NEON" has n = 4; Intel "AVX2" has n = 8; Intel "AVX-512" has n = 16; GPUs have larger *n*.

	flip-1	flops	
	insn fetch	insn fetch	
	flip-1	flops	
	insn decode	insn decode	
	flip-1	flops	
register read	register read	register read	register read
	flip-1	flops	l
		$\langle -$	
	flip-1	flops	
	register write	register write	

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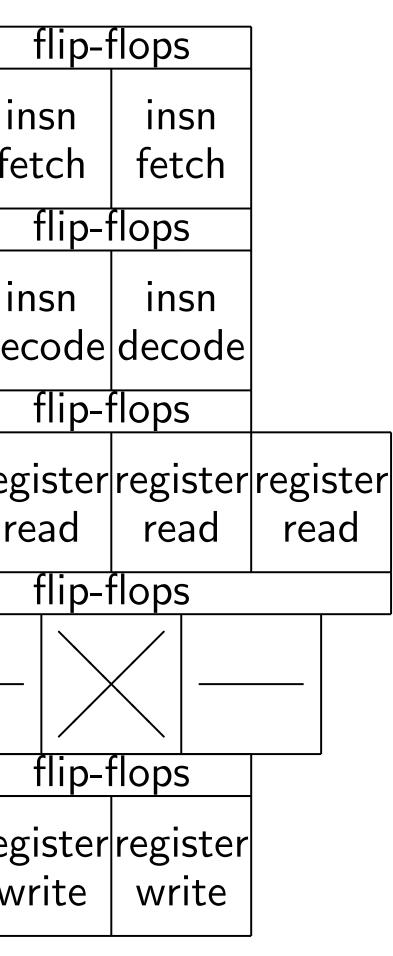
Benefit: Amortizes insn circuits.

		1	flip-1	flops	5		
		in fet	sn :ch	in fet			
		1	flip-1	flops	5		
		in dec	sn ode	in dec			
		1	flip-1	flops	5		
Ŭ	ster ad		ster ad		ster ad	regi rea	
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"Vector" processing: Expand each 32-bit integer into *n*-vector of 32-bit integers. ARM "NEON" has n = 4; Intel "AVX2" has n = 8; Intel "AVX-512" has n = 16; GPUs have larger n. $n \times$ speedup if $n \times$ arithmetic circuits, $n \times$ read/write circuits. Benefit: Amortizes insn circuits. Huge effect on higher-level

- algorithms and data structures.





"Vector" processing:

Expand each 32-bit integer into *n*-vector of 32-bit integers. ARM "NEON" has n = 4; Intel "AVX2" has n = 8; Intel "AVX-512" has n = 16; GPUs have larger n.

 $n \times$ speedup if $n \times$ arithmetic circuits, $n \times$ read/write circuits. Benefit: Amortizes insn circuits.

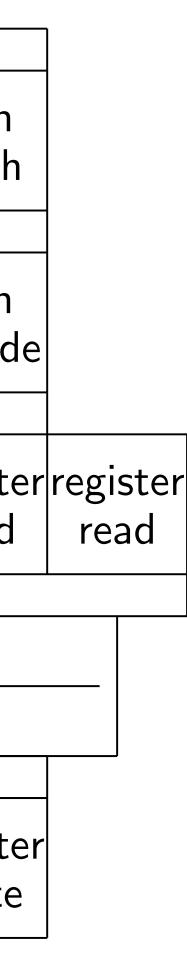
Huge effect on higher-level algorithms and data structures.

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Network on chip:

How expensive is a

Input: array of n r Each number in $\{$

represented in bina

Output: array of *i* in increasing order represented in bina same multiset as i

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Network on chip: the mesh

How expensive is sorting? Input: array of *n* numbers. Each number in $\{1, 2, \ldots, n\}$ represented in binary. Output: array of *n* numbers in increasing order, represented in binary; same multiset as input.

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Output: array of *n* numbers, in increasing order, represented in binary; same multiset as input.

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Metric: seconds used by circuit of area $n^{1+o(1)}$.

For simplicity assume $n = 4^k$.

processing:

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How expensive is sorting?

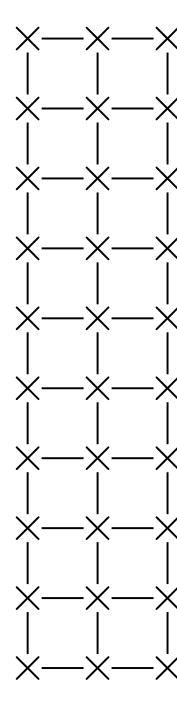
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<u>Network on chip: the mesh</u> How expensive is sorting?

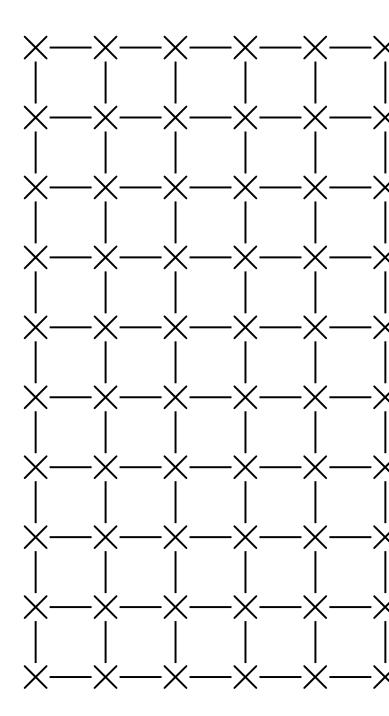
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Spread array across square mesh of n seach of area $n^{o(1)}$ with near-neighbor



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Network on chip: the mesh

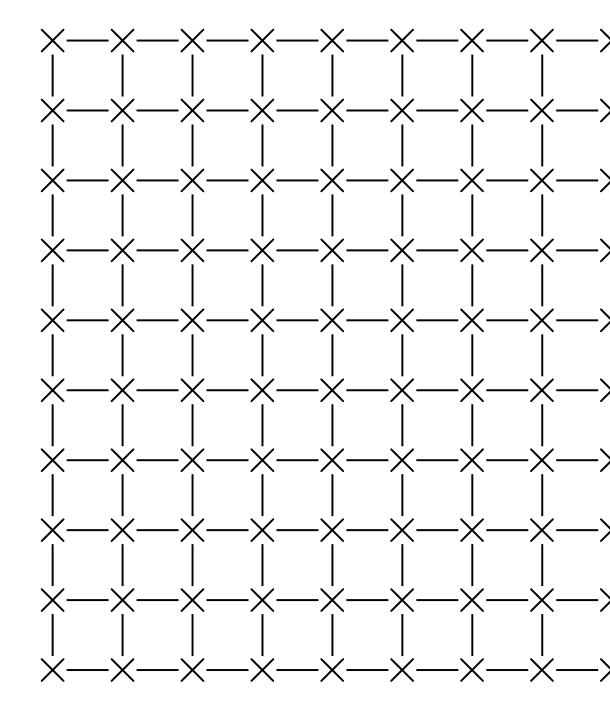
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Spread array across square mesh of *n* small cells each of area $n^{o(1)}$,

with near-neighbor wiring:

Network on chip: the mesh

How expensive is sorting?

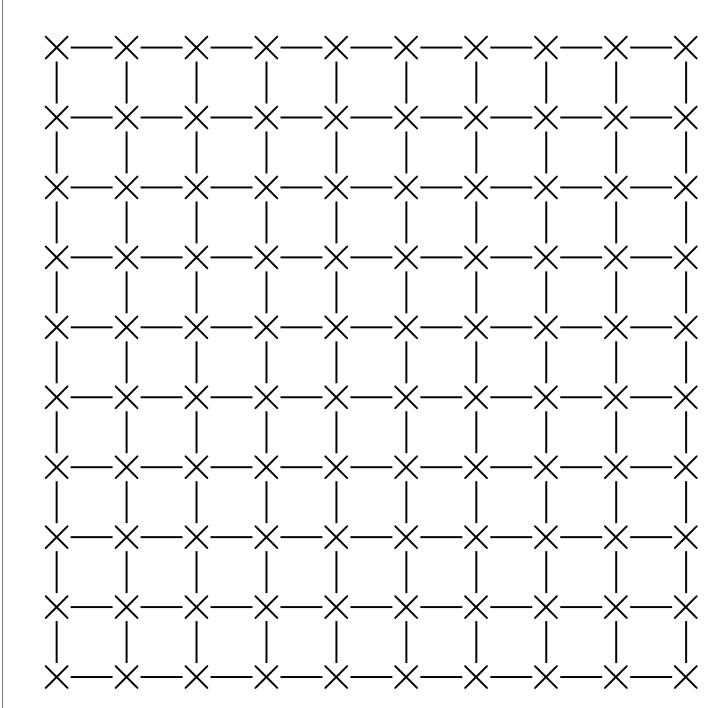
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Spread array across square mesh of *n* small cells, each of area $n^{o(1)}$, with near-neighbor wiring:

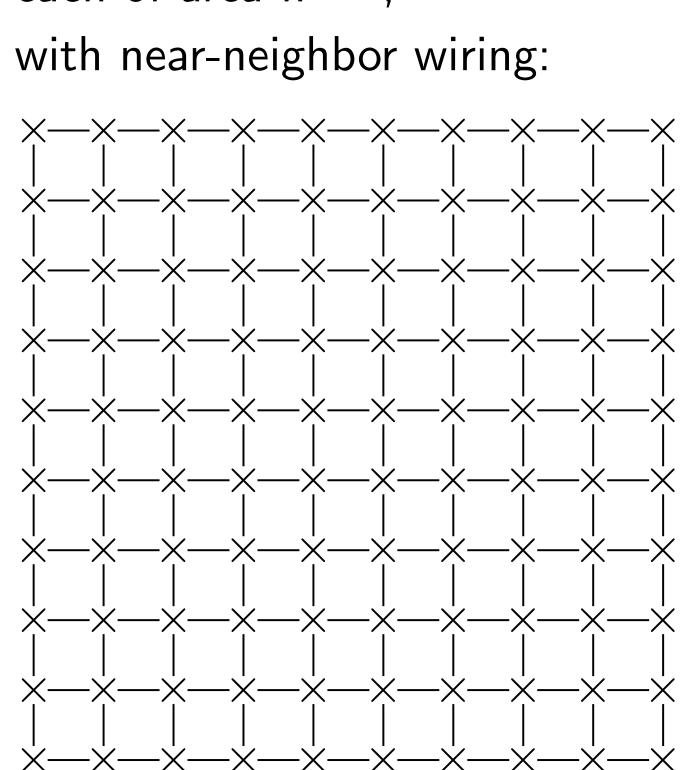


on chip: the mesh

- pensive is sorting?
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- array of *n* numbers, sing order,
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- seconds used by f area $n^{1+o(1)}$.

plicity assume $n = 4^k$.

Spread array across square mesh of *n* small cells, each of area $n^{o(1)}$, with near-neighbor wiring:



- Sort row in $n^{0.5+4}$
- Sort e
 - <u>31</u>4 1314
- Sort a
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- Repeated and the sequence of the

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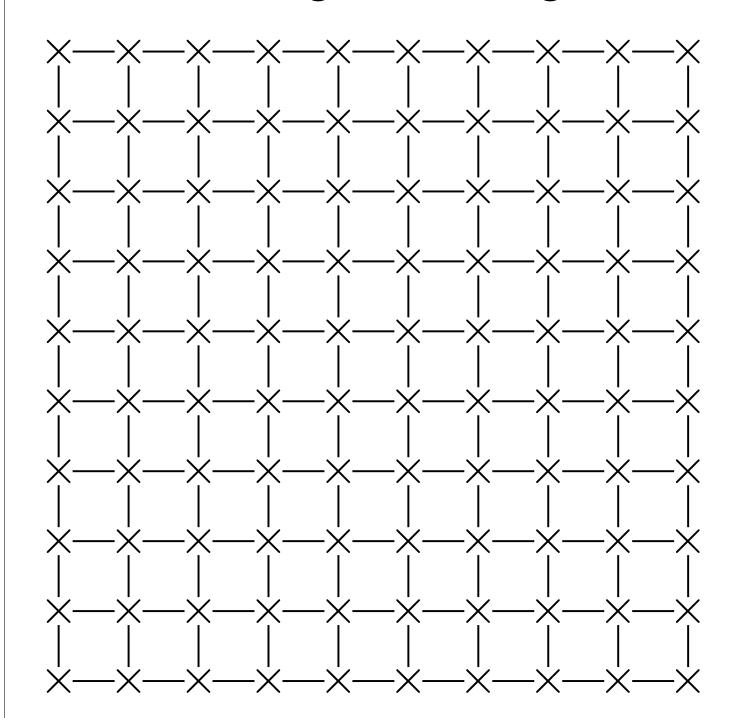
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me $n = 4^k$.

Spread array across square mesh of *n* small cells, each of area $n^{o(1)}$, with near-neighbor wiring:



Sort row of $n^{0.5}$ ce in $n^{0.5+o(1)}$ second

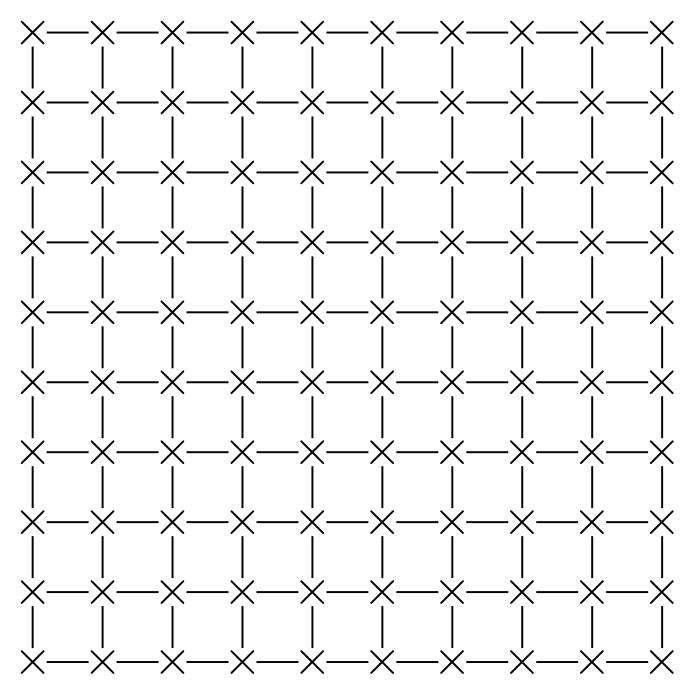
- Sort each pair in
 <u>31415926</u>
 13145926
- Sort alternate part of 1 3 1 4 5 9 2 6
 1 1 3 4 5 2 9 6
- Repeat until nur equals row lengt

Spread array across square mesh of *n* small cells, each of area $n^{o(1)}$,

with near-neighbor wiring:

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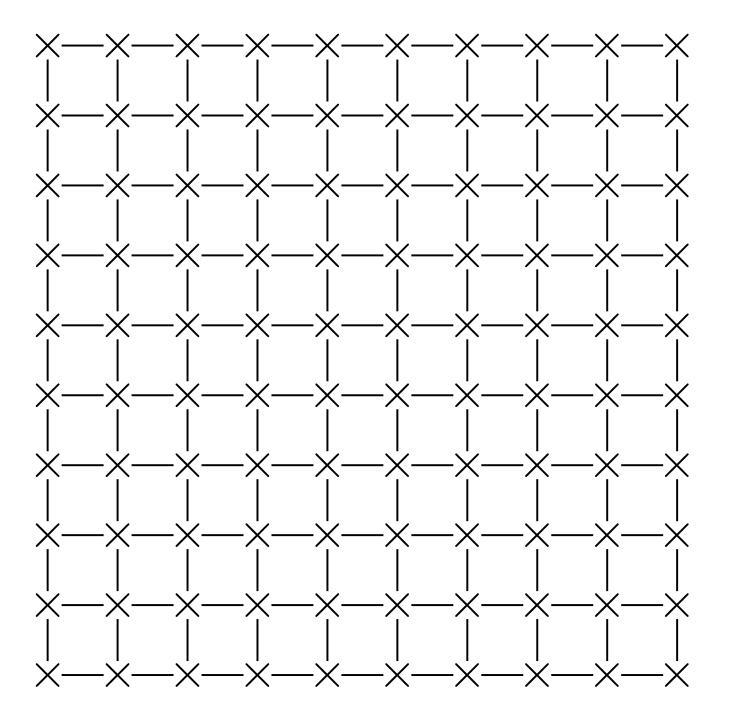
Sort row of $n^{0.5}$ cells in $n^{0.5+o(1)}$ seconds:

- Sort each pair in parallel. $3\ 1\ 4\ 1\ 5\ 9\ 2\ 6\mapsto$
- Sort alternate pairs in para $1 \underline{3} \underline{1} \underline{4} \underline{5} \underline{9} \underline{2} 6 \mapsto$
 - 11345296
- Repeat until number of st equals row length.

13145926

Spread array across square mesh of *n* small cells, each of area $n^{o(1)}$.

with near-neighbor wiring:

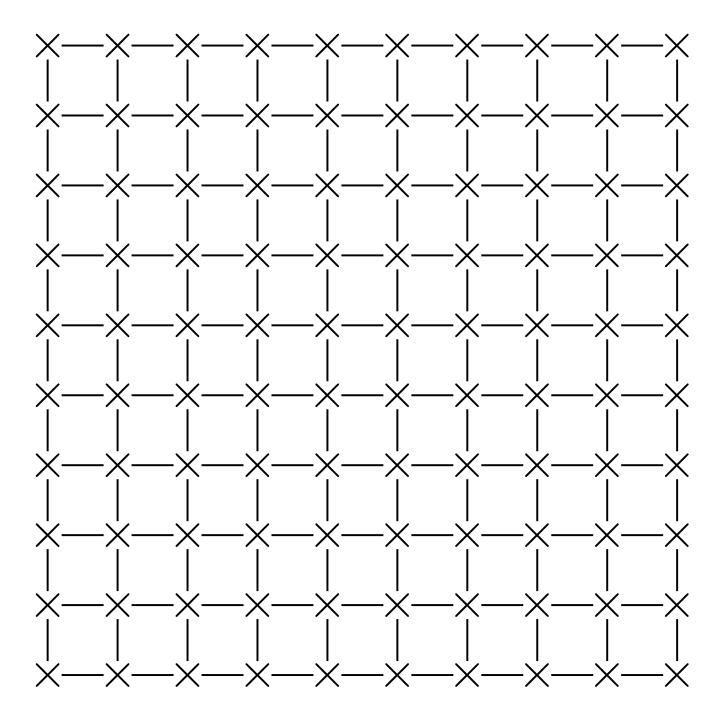


Sort row of $n^{0.5}$ cells in $n^{0.5+o(1)}$ seconds:

- Sort each pair in parallel. $3\ 1\ 4\ 1\ 5\ 9\ 2\ 6\mapsto$ 13145926
- Sort alternate pairs in parallel. $1 \underline{3} \underline{1} \underline{4} \underline{5} \underline{9} \underline{2} 6 \mapsto$ 11345296
- Repeat until number of steps equals row length.

Spread array across square mesh of *n* small cells, each of area $n^{o(1)}$.

with near-neighbor wiring:

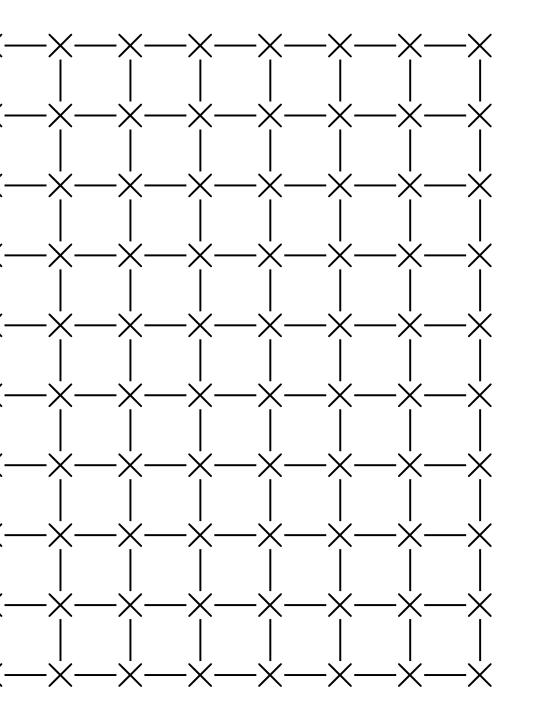


Sort row of $n^{0.5}$ cells in $n^{0.5+o(1)}$ seconds:

- Sort each pair in parallel. $3\ 1\ 4\ 1\ 5\ 9\ 2\ 6\mapsto$ 13145926
- Sort alternate pairs in parallel. $1 \underline{3} \underline{1} \underline{4} \underline{5} \underline{9} \underline{2} 6 \mapsto$ 11345296
- Repeat until number of steps equals row length.

Sort *each* row, in parallel, in a *total* of $n^{0.5+o(1)}$ seconds.

- array across
- nesh of *n* small cells, area $n^{o(1)}$,
- r-neighbor wiring:



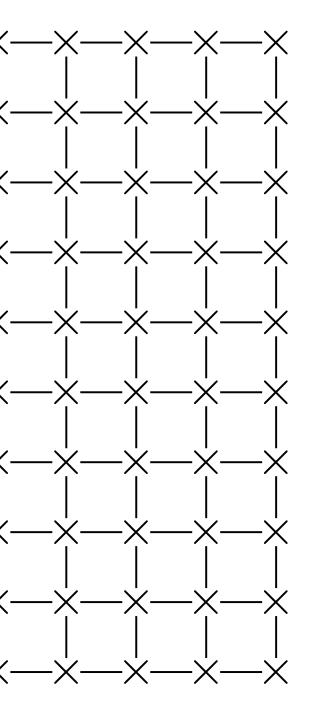
Sort row of $n^{0.5}$ cells in $n^{0.5+o(1)}$ seconds:

- Sort each pair in parallel. $\underline{31} \underline{41} \underline{59} \underline{26} \mapsto$ 13145926
- Sort alternate pairs in parallel. $1 \underline{3} \underline{1} \underline{4} \underline{5} \underline{9} \underline{2} 6 \mapsto$ 11345296
- Repeat until number of steps equals row length.

Sort *each* row, in parallel, in a *total* of $n^{0.5+o(1)}$ seconds.

- Sort all in $n^{0.5+6}$
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 - in para
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- small cells,
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Sort row of $n^{0.5}$ cells in $n^{0.5+o(1)}$ seconds:

- Sort each pair in parallel.
 <u>31415926</u> →
 13145926
- Sort alternate pairs in parallel.
 1 <u>3 1 4 5 9 2</u> 6 →
 1 1 3 4 5 2 9 6
- Repeat until number of steps equals row length.

Sort *each* row, in parallel, in a *total* of $n^{0.5+o(1)}$ seconds.

Sort all *n* cells in $n^{0.5+o(1)}$ second

- Recursively sort
 in parallel, if n >
- Sort each colum
- Sort each row in
- Sort each colum
- Sort each row in

With proper choice left-to-right/rightfor each row, can that this sorts who

```
Sort row of n^{0.5} cells
in n^{0.5+o(1)} seconds:
```

7

- Sort each pair in parallel. $\underline{31} \underline{41} \underline{59} \underline{26} \mapsto$ 13145926
- Sort alternate pairs in parallel. $1 \underline{31} \underline{45} \underline{92} 6 \mapsto$ 1 1 3 4 5 2 9 6
- Repeat until number of steps equals row length.

Sort *each* row, in parallel, in a *total* of $n^{0.5+o(1)}$ seconds.

- Recursively sort quadrants in parallel, if n > 1.
- Sort each column in parall
- Sort each row in parallel.
- Sort each column in parall
- Sort each row in parallel.
- With proper choice of left-to-right/right-to-left
- for each row, can prove
- that this sorts whole array.

Sort all *n* cells in $n^{0.5+o(1)}$ seconds:

Sort row of $n^{0.5}$ cells in $n^{0.5+o(1)}$ seconds:

- Sort each pair in parallel. $\underline{31} \underline{41} \underline{59} \underline{26} \mapsto$ 13145926
- Sort alternate pairs in parallel. $1 \underline{3} \underline{1} \underline{4} \underline{5} \underline{9} \underline{2} 6 \mapsto$ 11345296
- Repeat until number of steps equals row length.

Sort *each* row, in parallel, in a *total* of $n^{0.5+o(1)}$ seconds.

Sort all *n* cells in $n^{0.5+o(1)}$ seconds:

- Recursively sort quadrants in parallel, if n > 1.
- Sort each column in parallel.
- Sort each row in parallel.
- Sort each column in parallel.
- Sort each row in parallel.

With proper choice of left-to-right/right-to-left for each row, can prove that this sorts whole array.

of $n^{0.5}$ cells $o^{(1)}$ seconds:

- ach pair in parallel. $\underline{1} \ \underline{5} \ \underline{9} \ \underline{2} \ \underline{6} \mapsto$ 45926
- Iternate pairs in parallel. $\underline{45} \ \underline{92} \ 6 \mapsto$ 45296
- t until number of steps row length.
- h row, in parallel, al of $n^{0.5+o(1)}$ seconds.

Sort all *n* cells in $n^{0.5+o(1)}$ seconds:

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- Sort each column in parallel.
- Sort each row in parallel.
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- Sort each row in parallel.

With proper choice of left-to-right/right-to-left for each row, can prove that this sorts whole array.

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parallel, ^{o(1)} seconds. Sort all *n* cells in $n^{0.5+o(1)}$ seconds:

- Recursively sort quadrants in parallel, if n > 1.
- Sort each column in parallel.
- Sort each row in parallel.
- Sort each column in parallel.
- Sort each row in parallel.

With proper choice of left-to-right/right-to-left for each row, can prove that this sorts whole array.

For example, assumption 8×8 array is

3	1	4	1	5	9
5	3	5	8	9	7
2	3	8	4	6	2
3	3	8	3	2	7
0	2	8	8	4	1
1	6	9	3	9	9
5	1	0	5	8	2
7	4	9	4	4	5

```
Sort all n cells
in n^{0.5+o(1)} seconds:
```

- Recursively sort quadrants in parallel, if n > 1.
- Sort each column in parallel.
- Sort each row in parallel.
- Sort each column in parallel.
- Sort each row in parallel.

With proper choice of left-to-right/right-to-left for each row, can prove that this sorts whole array.

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For example, assume that

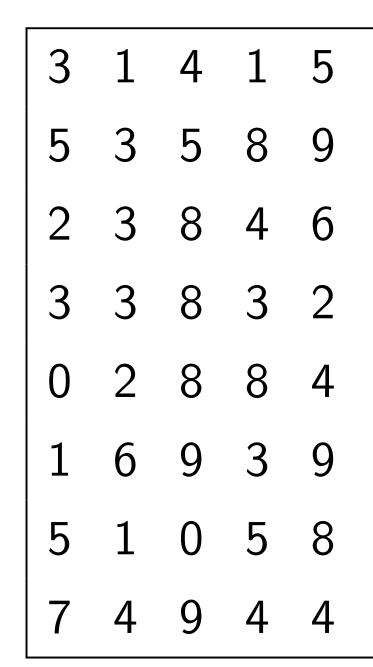
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	V	anay				

4	1	5	9	2	6
5	8	9	7	9	3
8	4	6	2	6	4
8	3	2	7	9	5
8	8	4	1	9	7
9	3	9	9	3	7
0	5	8	2	0	9
9	4	4	5	9	2

Sort all *n* cells in $n^{0.5+o(1)}$ seconds:

- Recursively sort quadrants in parallel, if n > 1.
- Sort each column in parallel.
- Sort each row in parallel.
- Sort each column in parallel.
- Sort each row in parallel.

With proper choice of left-to-right/right-to-left for each row, can prove that this sorts whole array. For example, assumption 8×8 array is

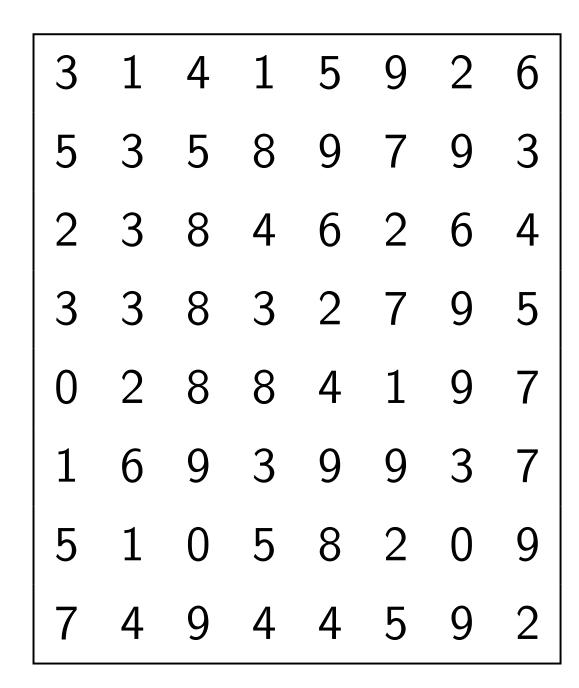


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S	in	cel	ls:

9	2	6
7	9	3
2	6	4
7	9	5
1	9	7
9	3	7
2	0	9
5	9	2

- *n* cells ²⁽¹⁾ seconds:
- sively sort quadrants
- allel, if n > 1.
- ach column in parallel.
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- ach column in parallel.
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- s sorts whole array.

For example, assume that this 8×8 array is in cells:



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1	1	2
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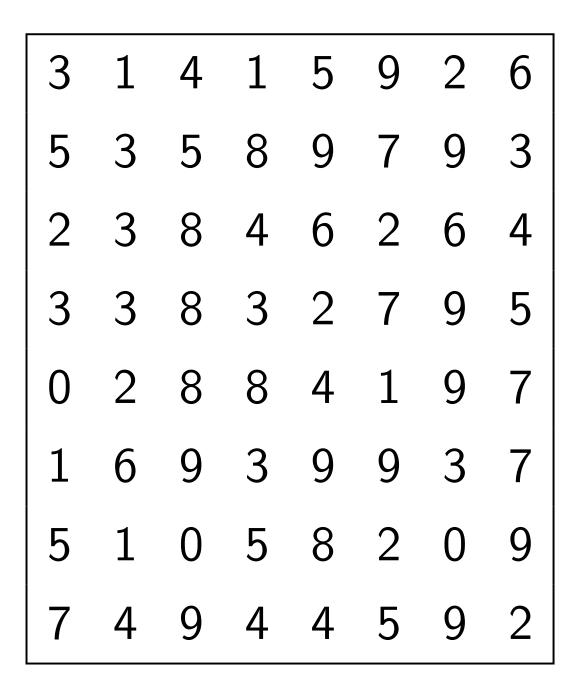
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ole array.

For example, assume that this 8×8 array is in cells:



Recursively sort quality top \rightarrow , bottom \leftarrow

1	1	2	3	2	2
3	3	3	3	4	5
3	4	4	5	6	6
5	8	8	8	9	9
1	1	0	0	2	2
4	4	3	2	5	4
7	6	5	5	9	8
9	9	8	8	9	9

For example, assume that this 8×8 array is in cells:

3	1	4	1	5	9	2	6
5	3	5	8	9	7	9	3
2	3	8	4	6	2	6	4
3	3	8	3	2	7	9	5
0	2	8	8	4	1	9	7
1	6	9	3	9	9	3	7
5	1	0	5	8	2	0	9
7	4	9	4	4	5	9	2

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Recursively sort quadrants, top \rightarrow , bottom \leftarrow :

2	3	2	2	2	3
3	3	4	5	5	6
4	5	6	6	7	7
8	8	9	9	9	9
0	0	2	2	1	0
3	2	5	4	4	3
5	5	9	8	7	7
8	8	9	9	9	9

For example, assume that this 8×8 array is in cells:

3	1	4	1	5	9	2	6
5	3	5	8	9	7	9	3
2	3	8	4	6	2	6	4
3	3	8	3	2	7	9	5
0	2	8	8	4	1	9	7
1	6	9	3	9	9	3	7
5	1	0	5	8	2	0	9
7	4	9	4	4	5	9	2

Recursively sort quadrants, top \rightarrow , bottom \leftarrow :

1	1	2	3	2	
3	3	3	3	4	
3	4	4	5	6	
5	8	8	8	9	
1	1	0	0	2	
4	4	3	2	5	
7	6	5	5	9	
9	9	8	8	9	

2	2	3
5	5	6
6	7	7
9	9	9
2	1	0
4	4	3
8	7	7
9	9	9

nple, assume that 8 array is in cells:

┣	1	5	9	2	6
-	8	9	7	9	3
3	4	6	2	6	4
3	3	2	7	9	5
3	8	4	1	9	7
)	3	9	9	3	7
)	5	8	2	0	9
)	4	4	5	9	2

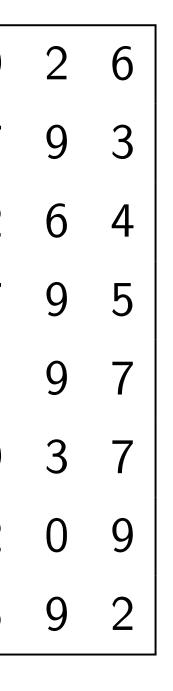
Recursively sort quadrants, top \rightarrow , bottom \leftarrow :

1	1	2	3	2	2	2	3
3	3	3	3	4	5	5	6
3	4	4	5	6	6	7	7
5	8	8	8	9	9	9	9
1	1	0	0	2	2	1	0
4	4	3	2	5	4	4	3
7	6	5	5	9	8	7	7
9	9	8	8	9	9	9	9

Sort eac

1	1	C
1	1	2
3	3	(1)
3	4	(1)
4	4	4
5	6	ц)
7	8	8
9	9	8

me that in cells:



Recursively sort quadrants, top \rightarrow , bottom \leftarrow :

1	1	2	3	2	2	2	3
3	3	3	3	4	5	2 5	6
3	4	4	5	6	6	7	7
5	8	8	8	9	9	9	9
1	1	0	0	2	2	1	0
4	4	3	2	5	4	4	3
7	6	5	5	9	8	7	7
9	9	8	8	9	9	9	9

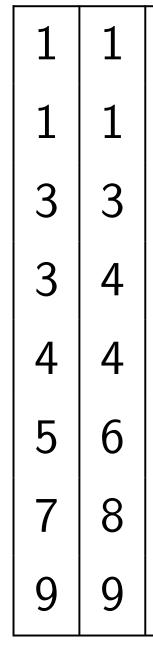
Sort each column in parallel:

1	1	0	0	2	2
1	1	2	2	2	2 2
3	3	3	3	4	4
3	4	3	3	5	5 6
4	4	4	5	6	6
5	6	5	5	9	8
7	8	8	8	9	9 9
9	9	8	8	9	9

Recursively sort quadrants, top \rightarrow , bottom \leftarrow :

1	1	2	3	2	2	2	3
3	3	3	3	4	5	5	6
3	4	4	5	6	6	7	7
5	8	8	8	9	9	9	9
1	1	0	0	2	2	1	0
4	4	3	2	5	4	4	3
7	6	5	5	9	8	7	7
9	9	8	8	9	9	9	9

in parallel:



Sort each column

0	0	2	2	1	0
2	2	2	2	2	3
3	3	4	4	4	3
3	3	5	5	5	6
4	5	6	6	7	7
5	5	9	8	7	7
8	8	9	9	9	9
8	8	9	9	9	9

Recursively sort quadrants, top \rightarrow , bottom \leftarrow :

1	1	2	3	2	2	2	3
3	3	3	3	4	5	5	6
3	4	4	5	6	6	7	7
5	8	8	8	9	9	9	9
1	1	0	0	2	2	1	0
4	4	3	2	5	4	4	3
7	6	5	5	9	8	7	7
9	9	8	8	9	9	9	9

Sort each column in parallel:

1		1	0	0	2	2	1	0
1		1	2	2	2	2	2	3
	3	3	3	3	4	4	4	3
	3	4	3	3	5	5	5	6
	1	4	4	5	6	6	7	7
5	-)	6	5	5	9	8	7	7
7	7	8	8	8	9	9	9	9
Ç)	9	8	8	9	9	9	9

ely sort quadrants, bottom \leftarrow :

	3	2	2	2	3
8	3	4	5	5	6
┣	5	6	6	7	7
3	8	9	9	9	9
)	0	2	2	1	0
3	2	5	4	4	3
•	5	9	8	7	7
8	8	9	9	9	9

Sort each column in parallel:

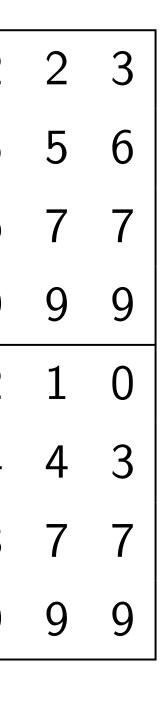
	1	1	0	0	2	2	1	0
	1	1	2	2	2	2	2	3
	3	3	3	3	4	4	4	3
	3	4	3	3	5	5	5	6
	4	4	4	5	6	6	7	7
	5	6	5	5	9	8	7	7
.	7	8	8	8	9	9	9	9
	9	9	8	8	9	9	9	9

Sort eac alternate

0	0	C
3	2	
3	3	(1)
6	5	С)
4	4	4
9	8	7
7	8	8
9	9	Ç

uadrants,

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Sort each column in parallel:

1	1	0	0	2	2	1	0
1	1	2	2	2	2	2	3
3	3	3	3	4	4	4	3
3	4	3	3	5	5	5	6
4	4	4	5	6	6	7	7
5	6	5	5	9	8	7	7
7	8	8	8	9	9	9	9
9	9	8	8	9	9	9	9

Sort each row in particular strength set of the set of

0	0	0	1	1	1
3	2	2	2	2	2
3	3	3	3	3	4
6	5	5	5	4	3
4	4	4	5	6	6
9	8	7	7	6	5
7	8	8	8	9	9
9	9	9	9	9	9

Sort each column in parallel:

1	1	0	0	2	2	1	0
1	1	2	2	2	2	2	3
3	3	3	3	4	4	4	3
3	4	3	3	5	5	5	6
4	4	4	5	6	6	7	7
5	6	5	5	9	8	7	7
7	8	8	8	9	9	9	9
9	9	8	8	9	9	9	9

Sort each row in parallel

Sort each row in parallel,							
alte	erna	atel	y	_, _	\rightarrow :		
0	0	0	1	1	1	2	2
3	2	2	2	2	2	1	1
3	3	3	3	3	4	4	4
6	5	5	5	4	3	3	3
4	4	4	5	6	6	7	7
9	8	7	7	6	5	5	5
7	8	8	8	9	9	9	9
9	9	9	9	9	9	8	8

Sort each column in parallel:

1	1	0	0	2	2	1	0
1	1	2	2	2	2	2	3
3	3	3	3	4	4	4	3
3	4	3	3	5	5	5	6
4	4	4	5	6	6	7	7
5	6	5	5	9	8	7	7
7	8	8	8	9	9	9	9
9	9	8	8	9	9	9	9

Sort each row in parallel, alternately \leftarrow , \rightarrow :

0	0	0	1	1	1	2	2
3	2	2	2	2	2	1	1
3	3	3	3	3	4	4	4
6	5	5	5	4	3	3	3
4	4	4	5	6	6	7	7
9	8	7	7	6	5	5	5
7	8	8	8	9	9	9	9
9	9	9	9	9	9	8	8
1							

h column

el:

0	2	2	1	0
2	2	2	2	3
3	4	4	4	3
3	5	5	5	6
5	6	6	7	7
5	9	8	7	7
8	9	9	9	9
8	9	9	9	9
	2 3 5 5 8	 2 3 4 3 5 6 5 9 8 9 	22343556565989	2222344355566759878999

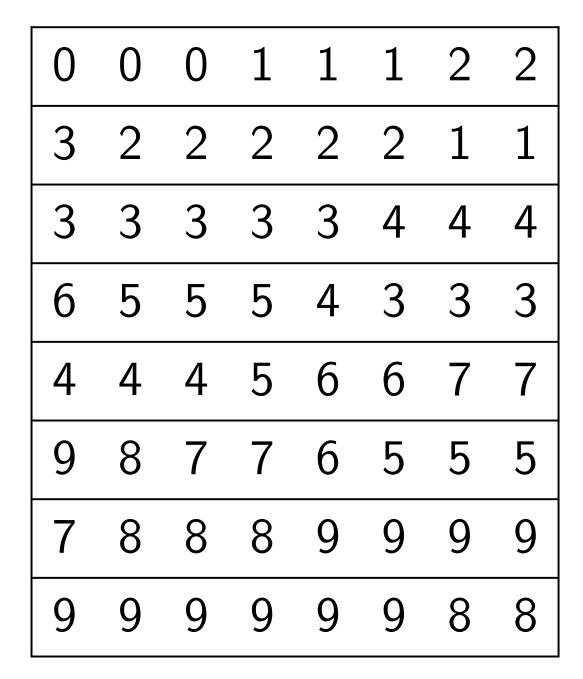
Sort each row in parallel, alternately \leftarrow , \rightarrow :

0	0	0	1	1	1	2	2
3	2	2	2	2	2	1	1
3	3	3	3	3	4	4	4
6	5	5	5	4	3	3	3
4	4	4	5	6	6	7	7
9	8	7	7	6	5	5	5
7	8	8	8	9	9	9	9
9	9	9	9	9	9	8	8

Sort eac

0	0	C
3	2	
3	3	(1)
4	4	4
6	5	Г)
7	8	7
9	8	8
9	9	Ç

Sort each row in parallel, alternately \leftarrow , \rightarrow :

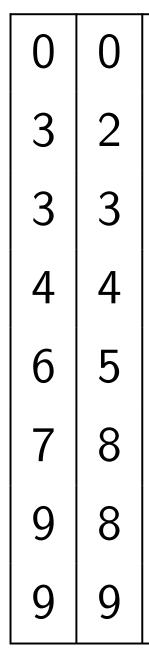


Sort each column in parallel:

		_	_		
0	0	0	1	1	1
3	2	2	2	2	23
3	3	3	3	3	3
4	4	4	5	4	4
6	5	5	5	6	5 6
7	8	7	7	6	6
9	8	8	8	9	9
9	9	9	9	9	9

Sort each row in parallel, alternately \leftarrow , \rightarrow :

in parallel:



Sort each column

0	1	1	1	1	1
2	2	2	2	2	2
3	3	3	3	3	3
4	5	4	4	4	4
5	5	6	5	5	5
7	7	6	6	7	7
8	8	9	9	8	8
9	9	9	9	9	9

Sort each row in parallel, alternately \leftarrow , \rightarrow :

Sort each column in parallel:

C)	0	0	1	1	1	1	1
	3	2	2	2	2	2	2	2
	3	3	3	3	3	3	3	3
	ŀ	4	4	5	4	4	4	4
6)	5	5	5	6	5	5	5
7	7	8	7	7	6	6	7	7
)	8	8	8	9	9	8	8
Ç)	9	9	9	9	9	9	9

h row in parallel,

ely
$$\leftarrow$$
, \rightarrow :

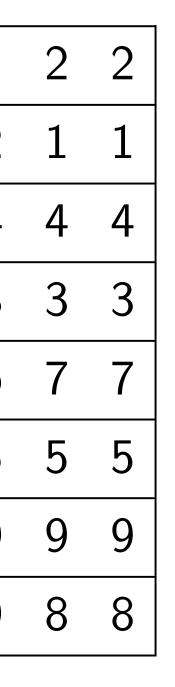
)	1	1	1	2	2
)	2	2	2	1	1
8	3	3	4	4	4
-	5	4	3	3	3
	5	6	6	7	7
7	7	6	5	5	5
	0	0	9	9	9
5	8	9	9	9	9
3)	8 9	9	9	9	8

Sort each column in parallel:

0	0	0	1	1	1	1	1
3	2	2	2	2	2	2	2
3	3	3	3	3	3	3	3
4	4	4	5	4	4	4	4
6	5	5	5	6	5	5	5
7	8	7	7	6	6	7	7
9	8	8	8	9	9	8	8
9	9	9	9	9	9	9	9

Sort eac							
or -	\rightarrow						
0	C						
2							
3	(1)						
4	Ц						
5	С)						
6	7						
8	8						
9	Ç						
	or - 0 2 3 4 5 6 8						

arallel,



Sort each column in parallel:

0	0	0	1	1	1	1	1
3	2	2	2	2	2	2	2
3	3	3	3	3	3	3	3
4	4	4	5	4	4	4	4
6	5	5	5	6	5	5	5
7	8	7	7	6	6	7	7
9	8	8	8	9	9	8	8
9	9	9	9	9	9	9	9

Sort each row in p									
<i>←</i>	or -	$\rightarrow a$	as c	lesi	reo				
0	0	0	1	1	1				
2	2	2	2	2	2				
3	3	3	3	3	3				
4	4	4	4	4	4				
5	5	5	5	5	5				
6	6	7	7	7	7				
8	8	8	8	8	9				
9	9	9	9	9	9				

Sort each column in parallel:

0	0	0	1	1	1	1	1
3	2	2	2	2	2	2	2
3	3	3	3	3	3	3	3
4	4	4	5	4	4	4	4
6	5	5	5	6	5	5	5
7	8	7	7	6	6	7	7
9	8	8	8	9	9	8	8
9	9	9	9	9	9	9	9

0	0	0	1	1	1	1	1
2	2	2	2	2	2	2	3
3	3	3	3	3	3	3	3
4	4	4	4	4	4	4	5
5	5	5	5	5	5	6	6
6	6	7	7	7	7	7	8
8	8	8	8	8	9	9	9
9	9	9	9	9	9	9	9

Sort each row in parallel, \leftarrow or \rightarrow as desired:

Sort each column in parallel:

0	0	0	1	1	1	1	1
3	2	2	2	2	2	2	2
3	3	3	3	3	3	3	3
4	4	4	5	4	4	4	4
6	5	5	5	6	5	5	5
7	8	7	7	6	6	7	7
9	8	8	8	9	9	8	8
9	9	9	9	9	9	9	9

Sort each row in parallel, \leftarrow or \rightarrow as desired:

0	0	0	1	1	
2	2	2	2	2	
3	3	3	3	3	
4	4	4	4	4	
5	5	5	5	5	
6	6	7	7	7	
8	8	8	8	8	
9	9	9	9	9	

1	1	1
2	2	3
3	3	3
4	4	5
5	6	6
7	7	8
9	9	9
9	9	9

h column

el:

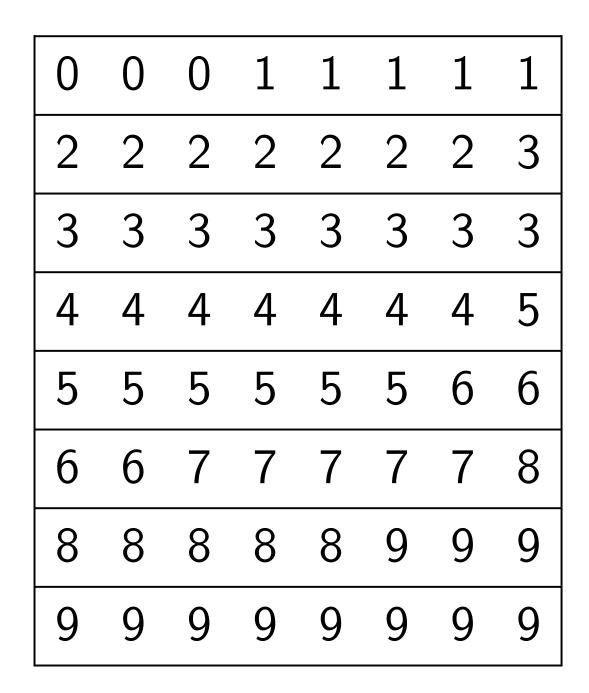
1	1	1	1	1
2	2	2	2	2
3	3	3	3	3
5	4	4	4	4
5	6	5	5	5
7	6	6	7	7
8	9	9	8	8
9	9	9	9	9
	2 3 5 7 8	 2 3 3 5 4 5 6 7 6 8 9 	22333354567689	222233335444565576678998

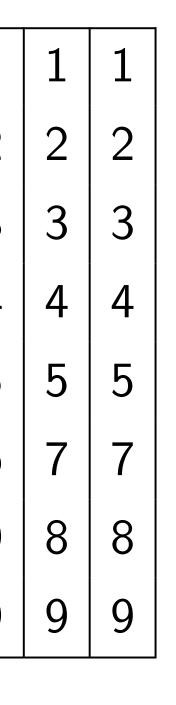
Sort each row in parallel, \leftarrow or \rightarrow as desired:

0	0	0	1	1	1	1	1
2	2	2	2	2	2	2	3
3	3	3	3	3	3	3	3
4	4	4	4	4	4	4	5
5	5	5	5	5	5	6	6
6	6	7	7	7	7	7	8
8	8	8	8	8	9	9	9
9	9	9	9	9	9	9	9

Chips ar towards parallelis GPUs: p Old Xeo New Xeo

Sort each row in parallel, \leftarrow or \rightarrow as desired:





Chips are in fact e towards having thi parallelism and co GPUs: parallel + Old Xeon Phi: par New Xeon Phi: par

Sort each row in parallel, \leftarrow or \rightarrow as desired:

0	0	1	1	1	1	1
2	2	2	2	2	2	3
3	3	3	3	3	3	3
4	4	4	4	4	4	5
5	5	5	5	5	6	6
6	7	7	7	7	7	8
8	8	8	8	9	9	9
9	9	9	9	9	9	9
	2 3 4 5 6 8	2 2 3 3 4 4 5 5 6 7 8 8	2 2 2 3 3 3 4 4 4 5 5 5 6 7 7 8 8 8	2 2 2 2 3 3 3 3 4 4 4 4 5 5 5 5 6 7 7 7 8 8 8 8	2 2 2 2 2 3 3 3 3 3 4 4 4 4 4 5 5 5 5 5 6 7 7 7 7 8 8 8 8 9	2 2 2 2 2 2 3 3 3 3 3 3 4 4 4 4 4 5 5 5 5 6 6 7 7 7 7 8 8 8 8 9 9

Chips are in fact evolving towards having this much parallelism and communicat GPUs: parallel + global RA Old Xeon Phi: parallel + rin New Xeon Phi: parallel + m Sort each row in parallel, \leftarrow or \rightarrow as desired:

$\begin{array}{cccccccccccccccccccccccccccccccccccc$								
3 3 3 3 3 3 3 3 4 4 4 4 4 4 5 5 5 5 5 5 6 6 6 6 7 7 7 7 8 8 8 8 8 9 9 9	0	0	0	1	1	1	1	1
4 4 4 4 4 4 5 5 5 5 5 5 6 6 6 6 7 7 7 7 8 8 8 8 8 8 9 9 9	2	2	2	2	2	2	2	3
5 5 5 5 5 6 6 6 6 7 7 7 7 8 8 8 8 8 9 9 9	3	3	3	3	3	3	3	3
6 6 7 7 7 7 8 8 8 8 8 9 9 9	4	4	4	4	4	4	4	5
8 8 8 8 8 9 9 9	5	5	5	5	5	5	6	6
	6	6	7	7	7	7	7	8
99999999	8	8	8	8	8	9	9	9
	9	9	9	9	9	9	9	9

Chips are in fact evolving towards having this much parallelism and communication.

GPUs: parallel + global RAM. Old Xeon Phi: parallel + ring. New Xeon Phi: parallel + mesh.

Sort each row in parallel, \leftarrow or \rightarrow as desired:

0	0	0	1	1	1	1	1
2	2	2	2	2	2	2	3
3	3	3	3	3	3	3	3
4	4	4	4	4	4	4	5
5	5	5	5	5	5	6	6
6	6	7	7	7	7	7	8
8	8	8	8	8	9	9	9
9	9	9	9	9	9	9	9
					-		

Chips are in fact evolving towards having this much parallelism and communication.

GPUs: parallel + global RAM.Old Xeon Phi: parallel + ring.New Xeon Phi: parallel + mesh.

Algorithm designers don't even get the right exponent without taking this into account.

evolving his much ommunication. global RAM. arallel + ring. barallel + mesh

Sort each row in parallel, \leftarrow or \rightarrow as desired:

0	0	0	1	1	1	1	1
2	2	2	2	2	2	2	3
3	3	3	3	3	3	3	3
4	4	4	4	4	4	4	5
5	5	5	5	5	5	6	6
6	6	7	7	7	7	7	8
8	8	8	8	8	9	9	9
9	9	9	9	9	9	9	9

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Shock waves into high levels of domain-specific algorithm design: e.g., for "NFS" factorization, replace "sieving" with "ECM".

h row in parallel, as desired:

1		1	1	1	1	
	–	–	–	–	–	
	2	2	2	2	3	
	3	3	3	3	3	
	4	4	4	4	5	
	5	5	5	6	6	
	7	7	7	7	8	
	8	8	9	9	9	
	9	9	9	9	9	

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At this p say, "Bu P, and a will proc "No, the would h (much n we have be unrel alternati class of far bette arallel,

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1	3	3	5	6	8	9	9
1	2	3	4	6	7	9	9

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The future of com

At this point man say, "But he should P, and an optimiz will produce Q." "No, the optimizing would have to be (much more so th we have now) that be unreliable." I h alternative to prop class of software v far better. . . .

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The future of compilers

At this point many readers say, "But he should only wr P, and an optimizing compil will produce Q." To this I sa "No, the optimizing compile would have to be so complie (much more so than anythir we have now) that it will in be unreliable." I have anoth alternative to propose, a new class of software which will far better. . . .

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oarallel + global RAM. n Phi: parallel + ring. on Phi: parallel + mesh.

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For 15 years or so I have be trying to think of how to wr compiler that really produce quality code. For example, I of the Mix programs in my are considerably more efficie than any of today's most vis compiling schemes would be to produce. I've tried to stu various techniques that a ha coder like myself uses, and t them into some systematic a automatic system. A few ye ago, several students and I at a typical sample of FOR7

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For 15 years or so I have been trying to think of how to write a compiler that really produces top quality code. For example, most of the Mix programs in my books are considerably more efficient than any of today's most visionary compiling schemes would be able to produce. I've tried to study the various techniques that a handcoder like myself uses, and to fit them into some systematic and automatic system. A few years ago, several students and I looked at a typical sample of FORTRAN

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programs [51], and hard to see how a could produce cod compete with our optimized object p found ourselves al up against the sar compiler needs to with the programr know properties of whether certain ca etc. And we could good language in such a dialog.

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For som me) had optimiza always r the-scen in the m the prog to know lifted fro ran acro [42] tha should b optimizi its optin language I have been how to write a ly produces top example, most ms in my books nore efficient 's most visionary s would be able ried to study the that a handuses, and to fit stematic and A few years nts and I looked e of FORTRAN

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