Cache-timing attacks

D. J. Bernstein

Thanks to:
University of Illinois at Chicago
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Alfred P. Sloan Foundation

http://cr.yp.to/papers.html#cachetiming, 2005:

“This paper reports successful extraction of a complete AES key from a network server on another computer. The targeted server used its key solely to encrypt data using the OpenSSL AES implementation on a Pentium III.”

All code included in paper.
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Most obvious timing variability: skipping an operation is faster than doing it.

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   for (i = 0
     if (x[i]
       return
   return 1;
```

New:

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   diff = 0;
   for (i = 0
     diff |= x
   return !di
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Solution: Use constant-time password comparison.

Old:

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for (i = 0;i < n;++i)
  if (x[i] != y[i])
    return 0;
return 1;
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New:

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diff = 0;
for (i = 0;i < n;++i)
  diff |= x[i] ^ y[i];
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AES has functions S, S' mapping bytes to bytes. Attack is against S' computed as follows:

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byte Sprime(byte b) {
  byte c = S(b);
  if (c<128) return c+c;
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CPUs handle this
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Reading from cached line takes less time than reading from uncached line.

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Uses table lookup and ⊕ (xor):

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`tab[k[0]`⊕`n[0]]`⊕`k[0]`⊕`e0`

etc.

$\mathrm{AES}_k(n) = (\texttt{e784}, \ldots, \texttt{e799})$.

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High-speed AES uses 4-byte registers, several 1024-byte tables. Operations: byte extraction (4 bytes to 1 byte), table lookup (1 byte to 4 byte), ⊕.

Attacker can force selected table entries out of L2 cache, observe encryption time.
Each cache miss creates timing signal, clearly visible despite noise from other AES cache misses, other software, etc.
Repeat for many plaintexts, easily deduce key.

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Example: `tab[k[0]` $\oplus$ `n[0]]` costs hundreds of extra cycles if this `tab` entry is not in L2 cache.

Knock `tab[13]` out of cache. See signal when $k[0] \oplus n[0] = 13$. Deduce $k[0]$ as $n[0] \oplus 13$. (Complication: cache lines; need more work to find bottom bits of $k[0]$.)

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What if computer has no browser, no buffer overflows, etc.? Clearly still possible to carry out the attack from another computer by figuring out packets that, when sent to (e.g.) Linux kernel, cause accesses of appropriate memory locations. Nobody has done this! Would make a nice paper!

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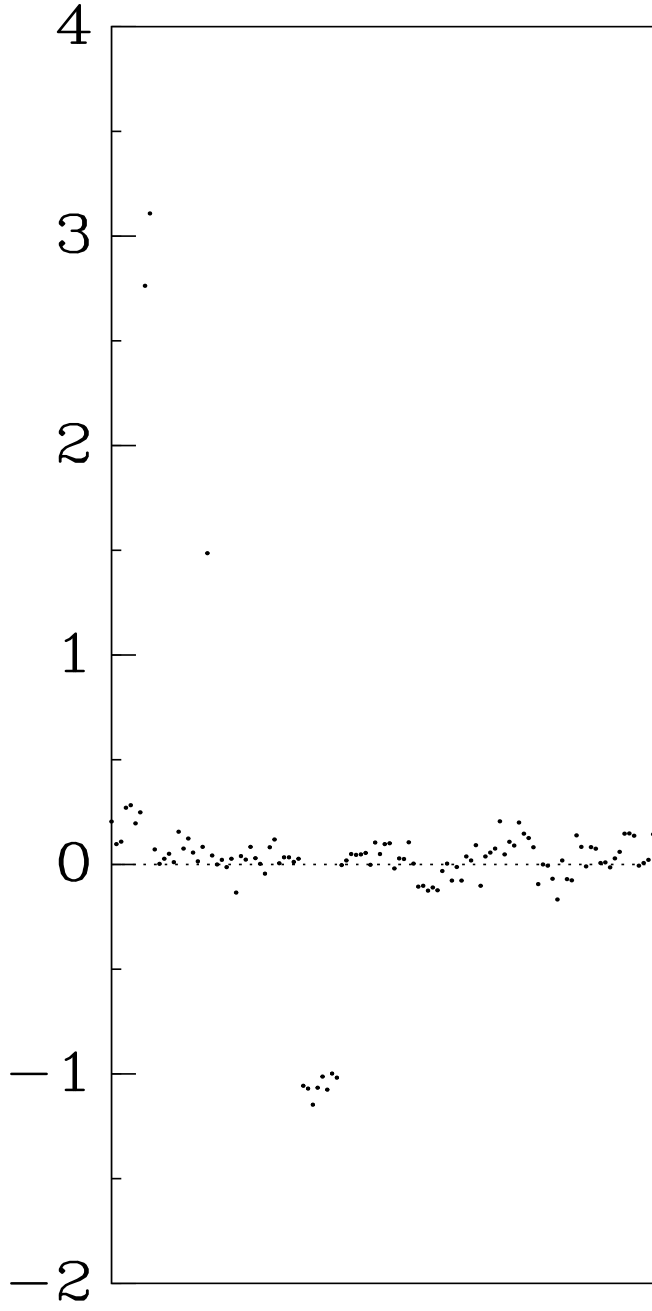

6. Breaking AES in cache

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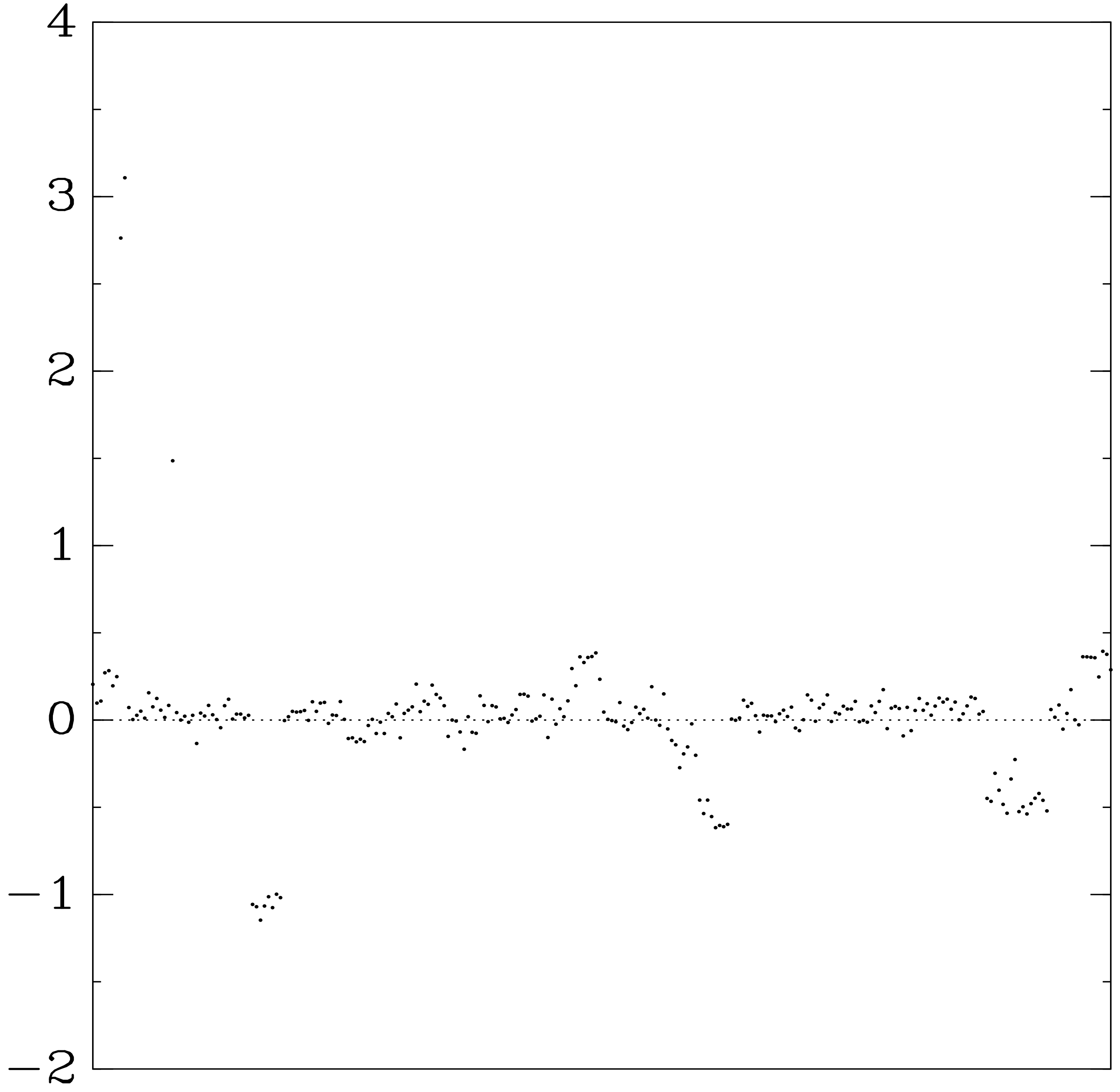

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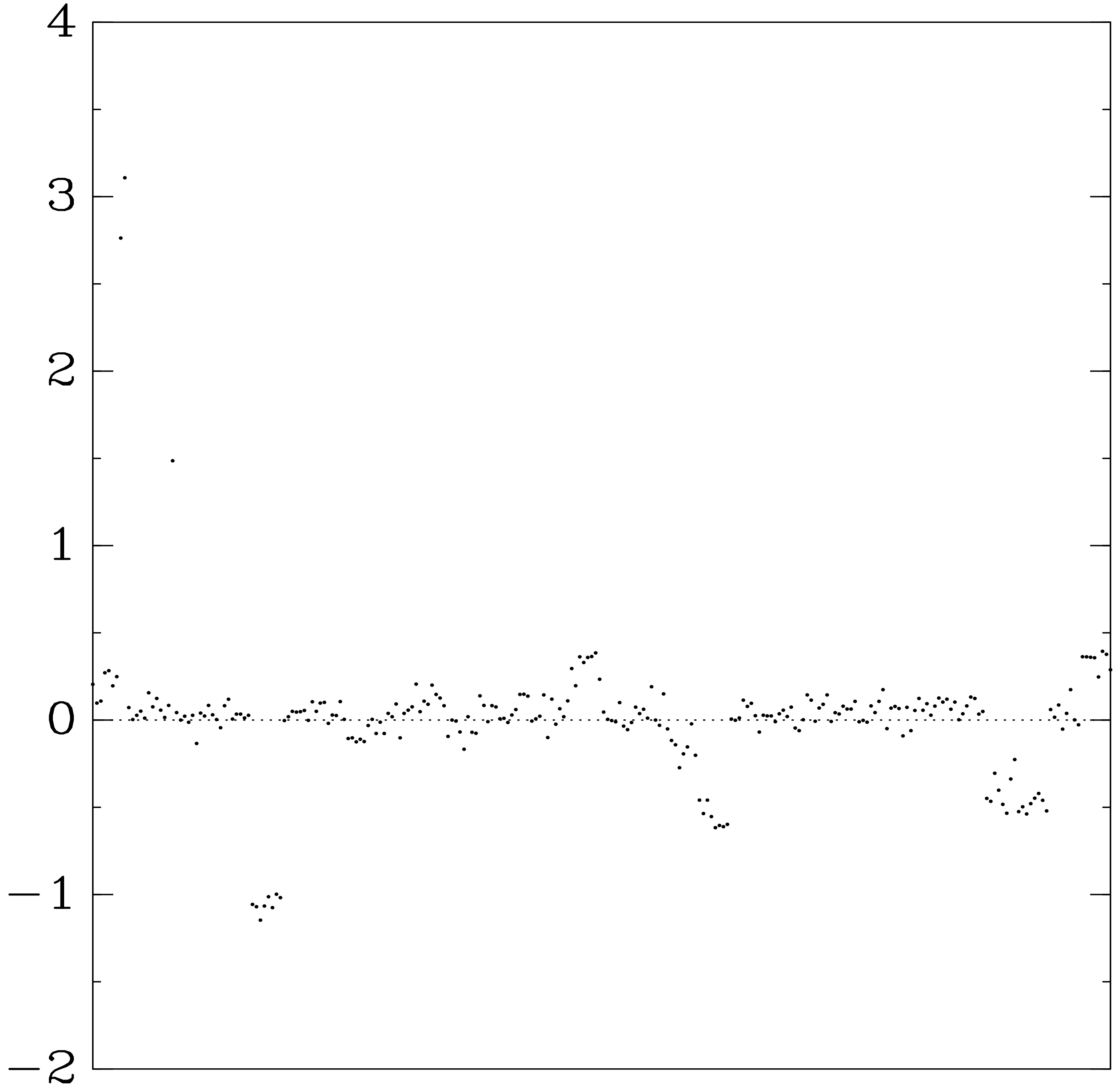

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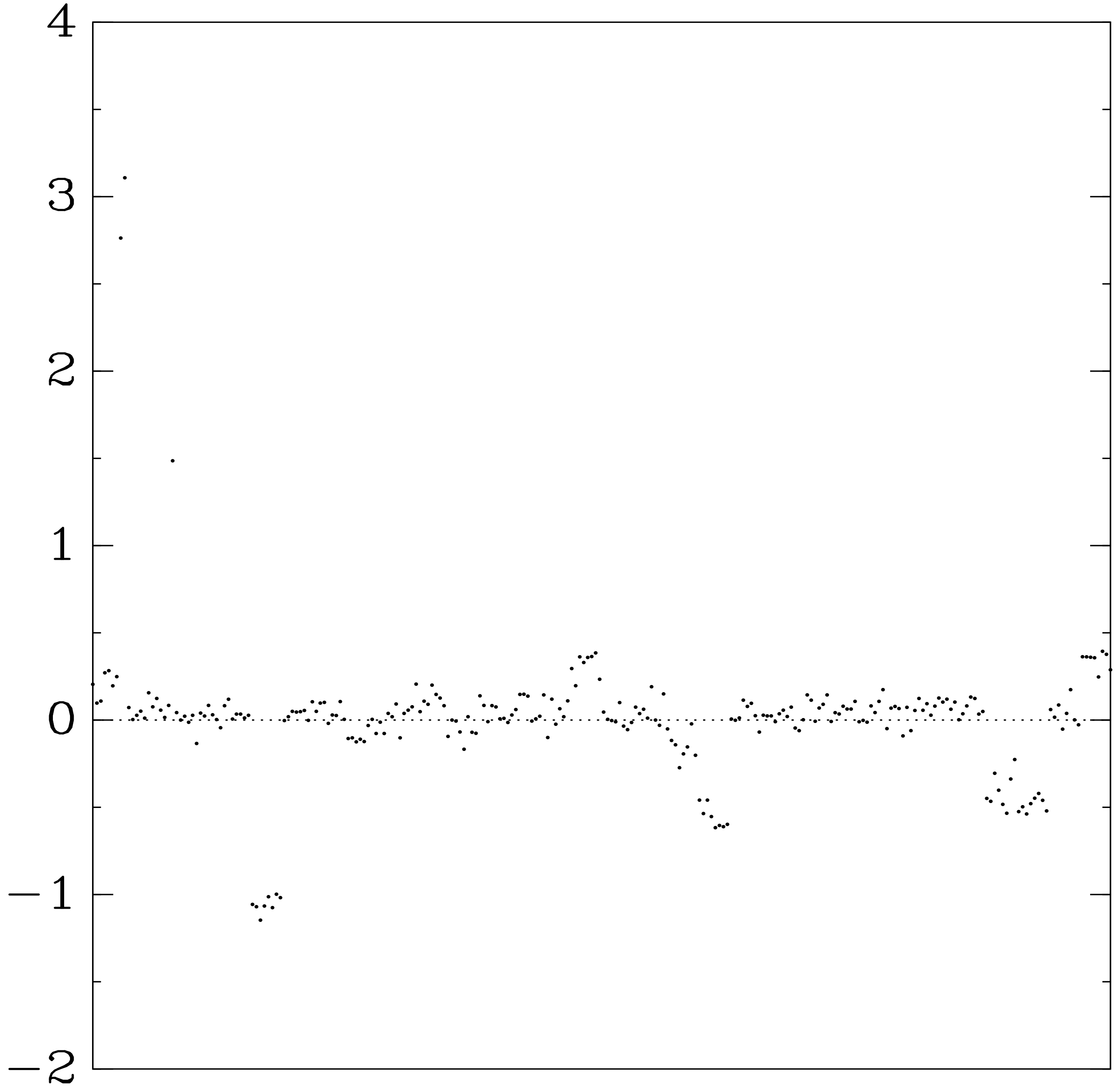
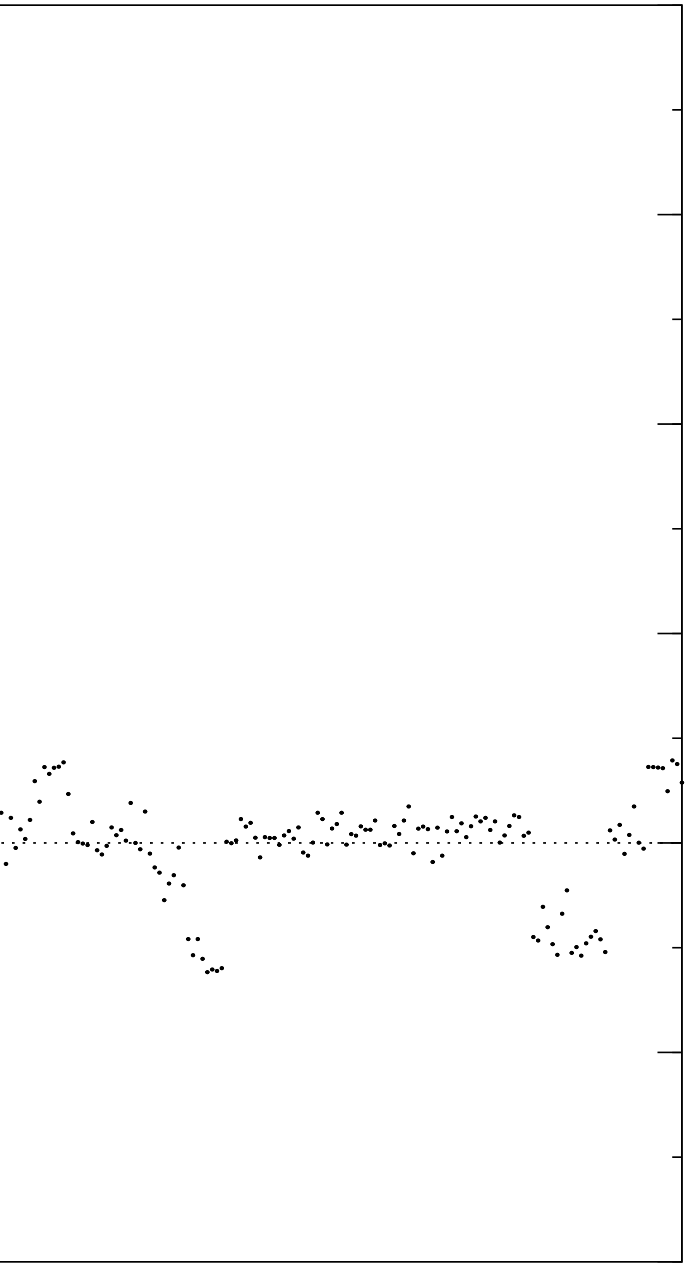


Graph has x-coordinates 0 through 255.

y-coordinate: average cycles to encrypt random plaintext with $k[13] \oplus n[13] = x$, minus average cycles to encrypt unrestricted random plaintext.

Encryption time (for this test code, this CPU, etc.) is maximized when $k[13] \oplus n[13] = 8$. 3-cycle signal.



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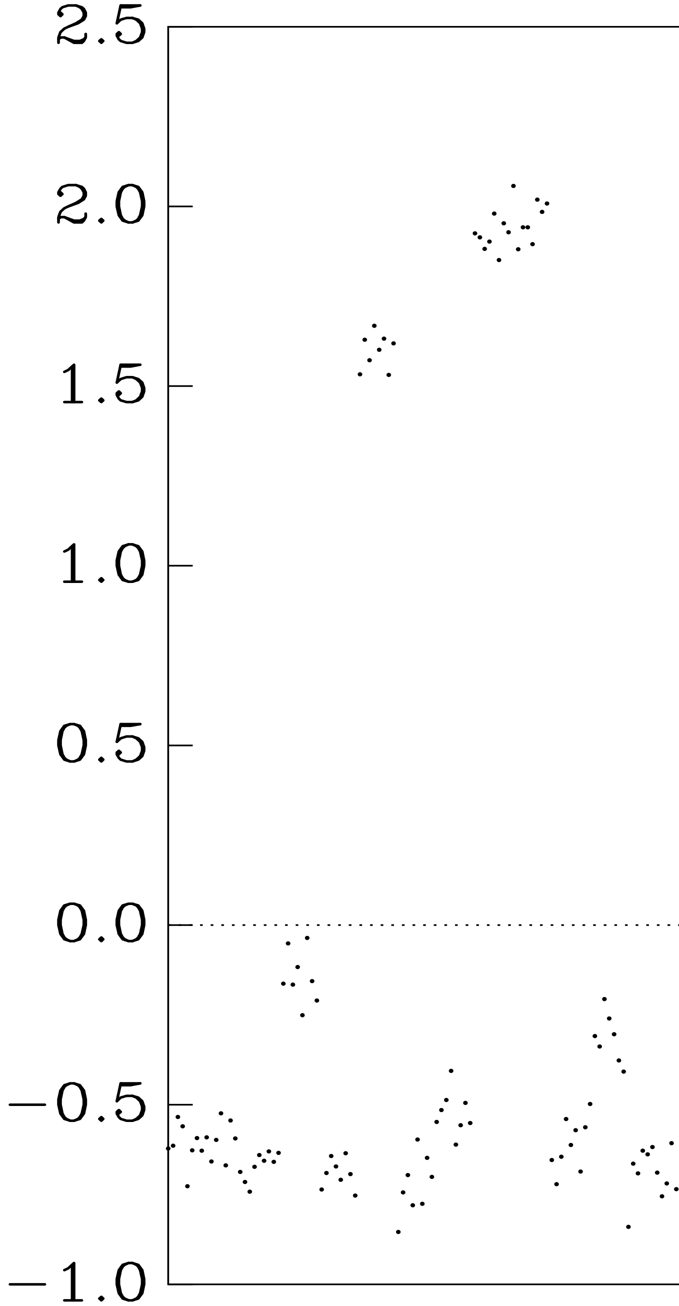

Graph for $k[5] \oplus$

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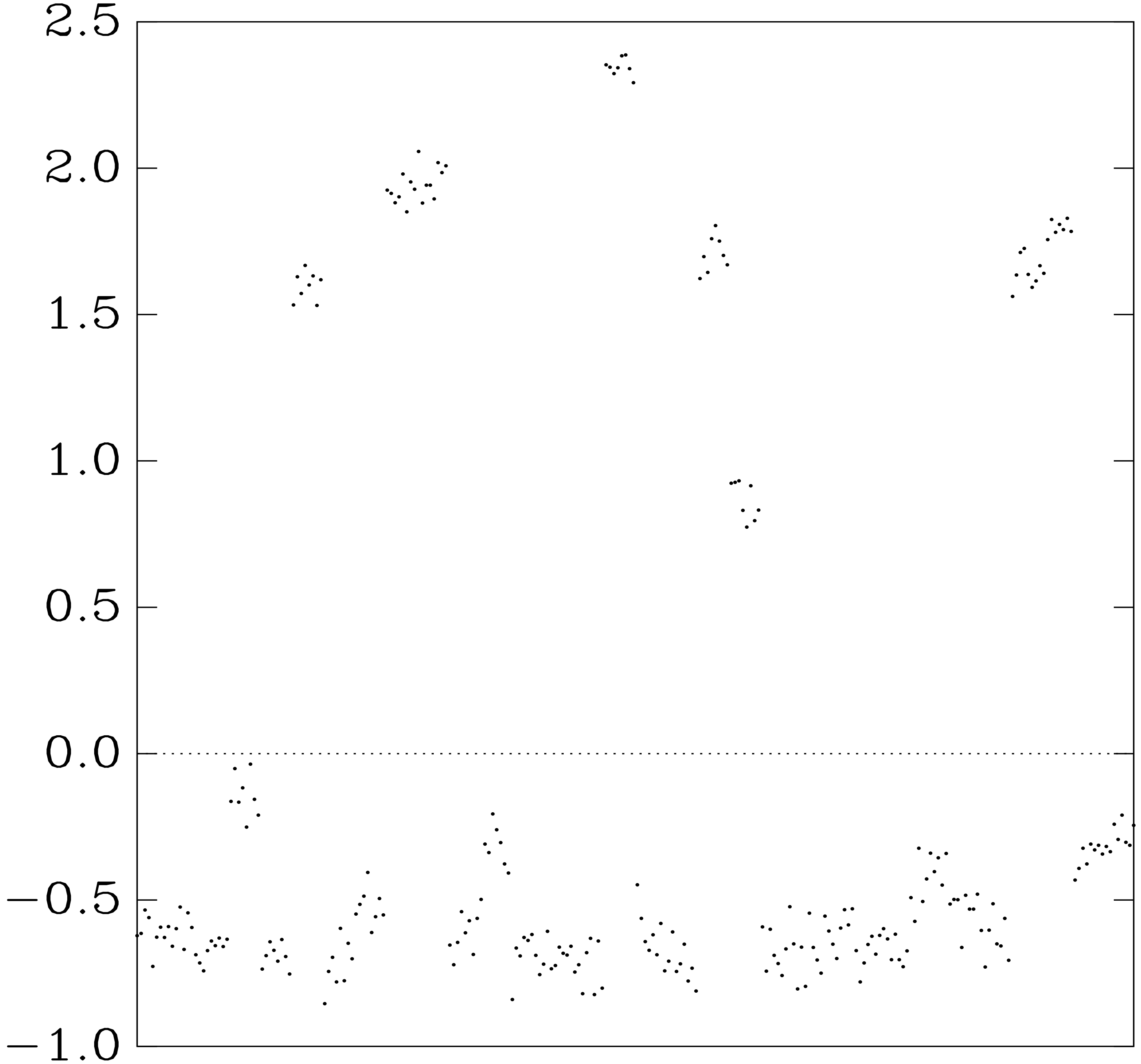

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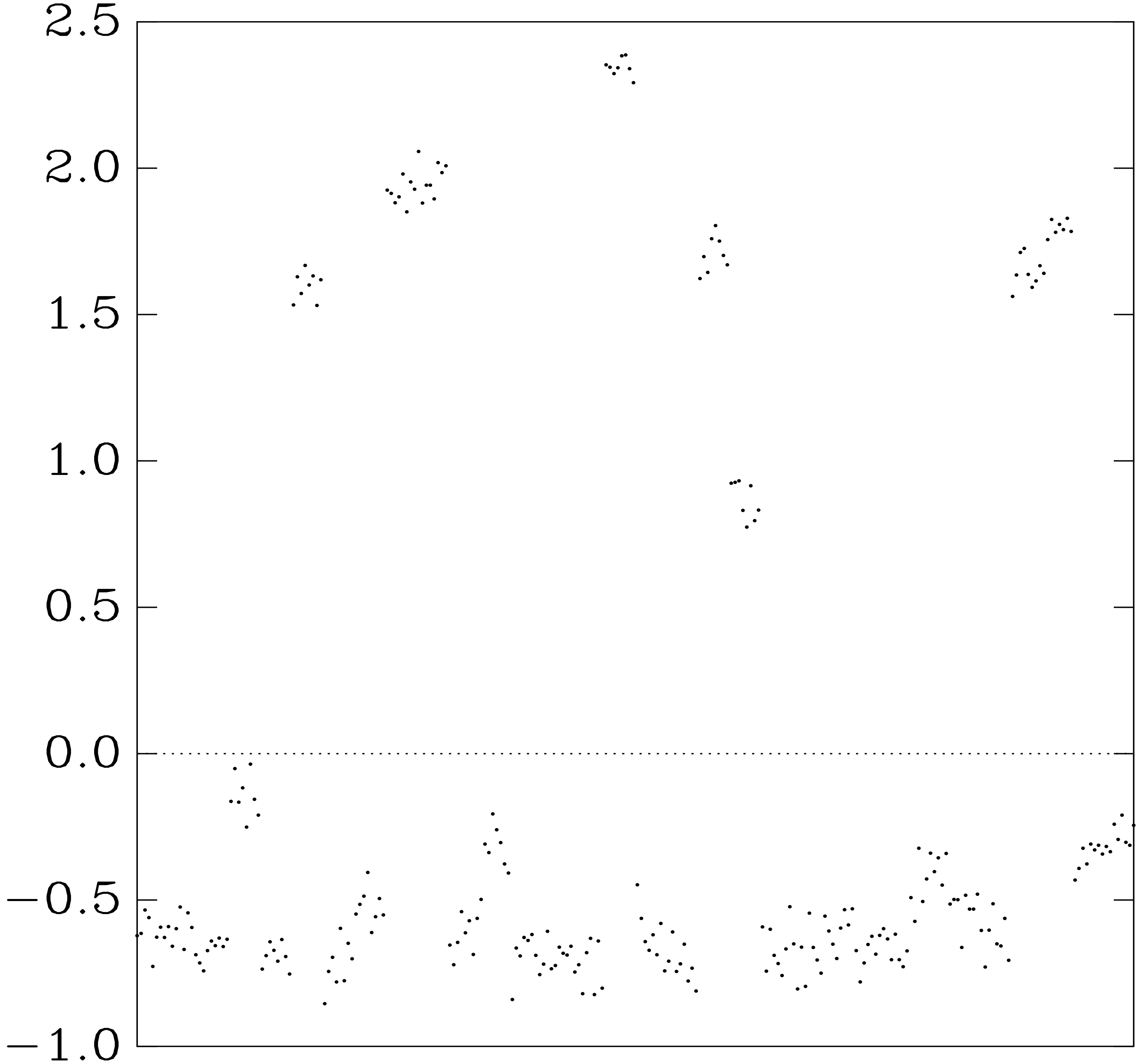

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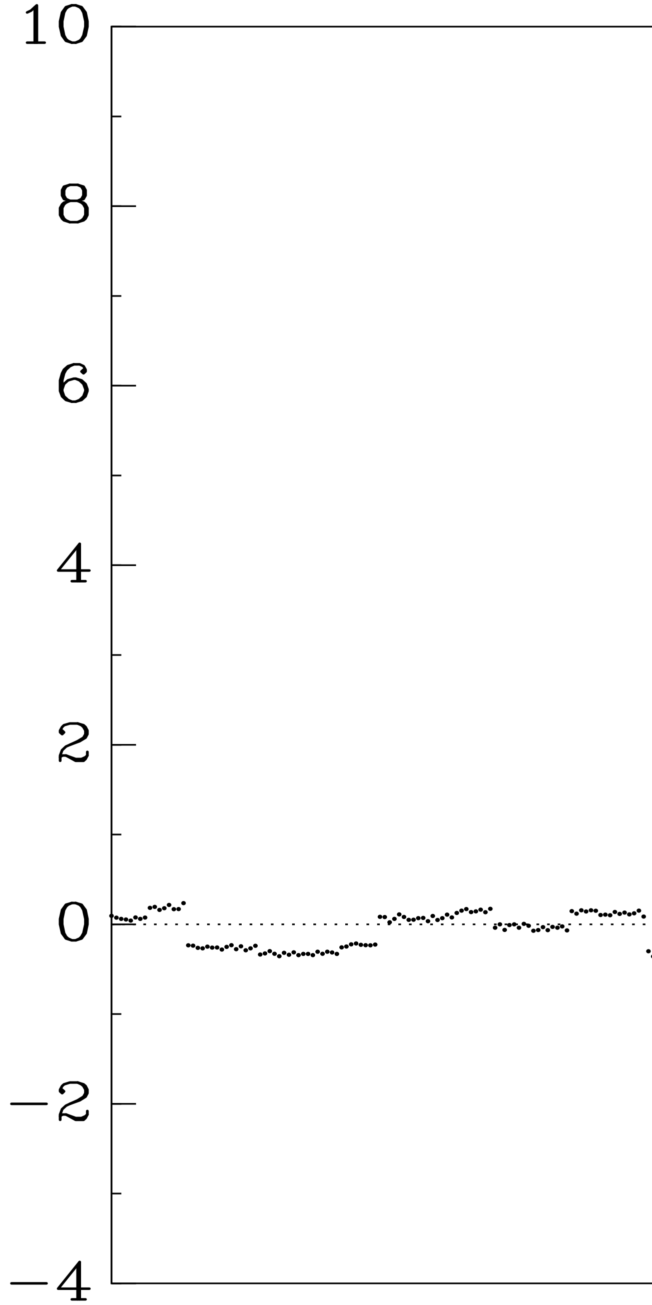

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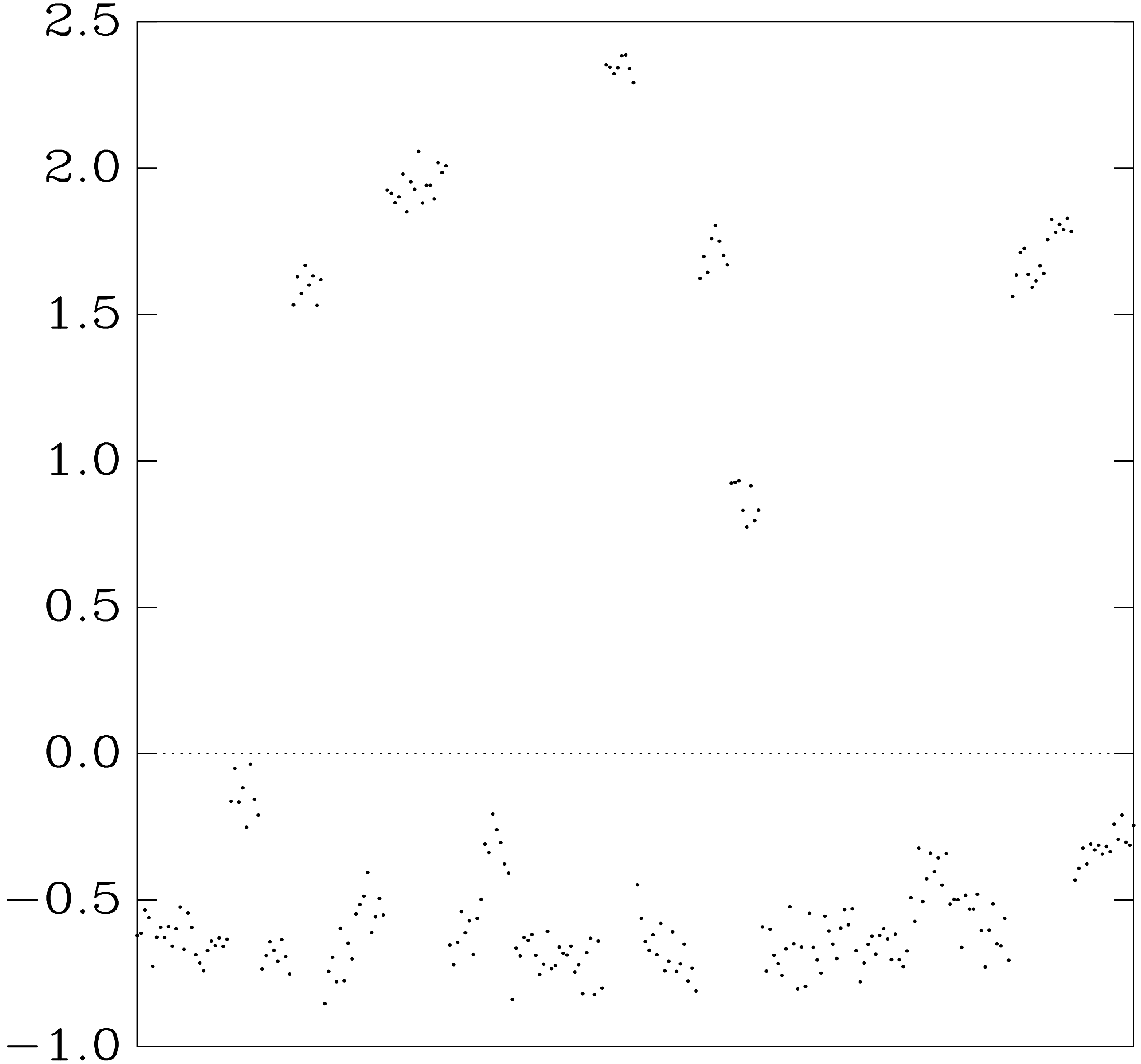

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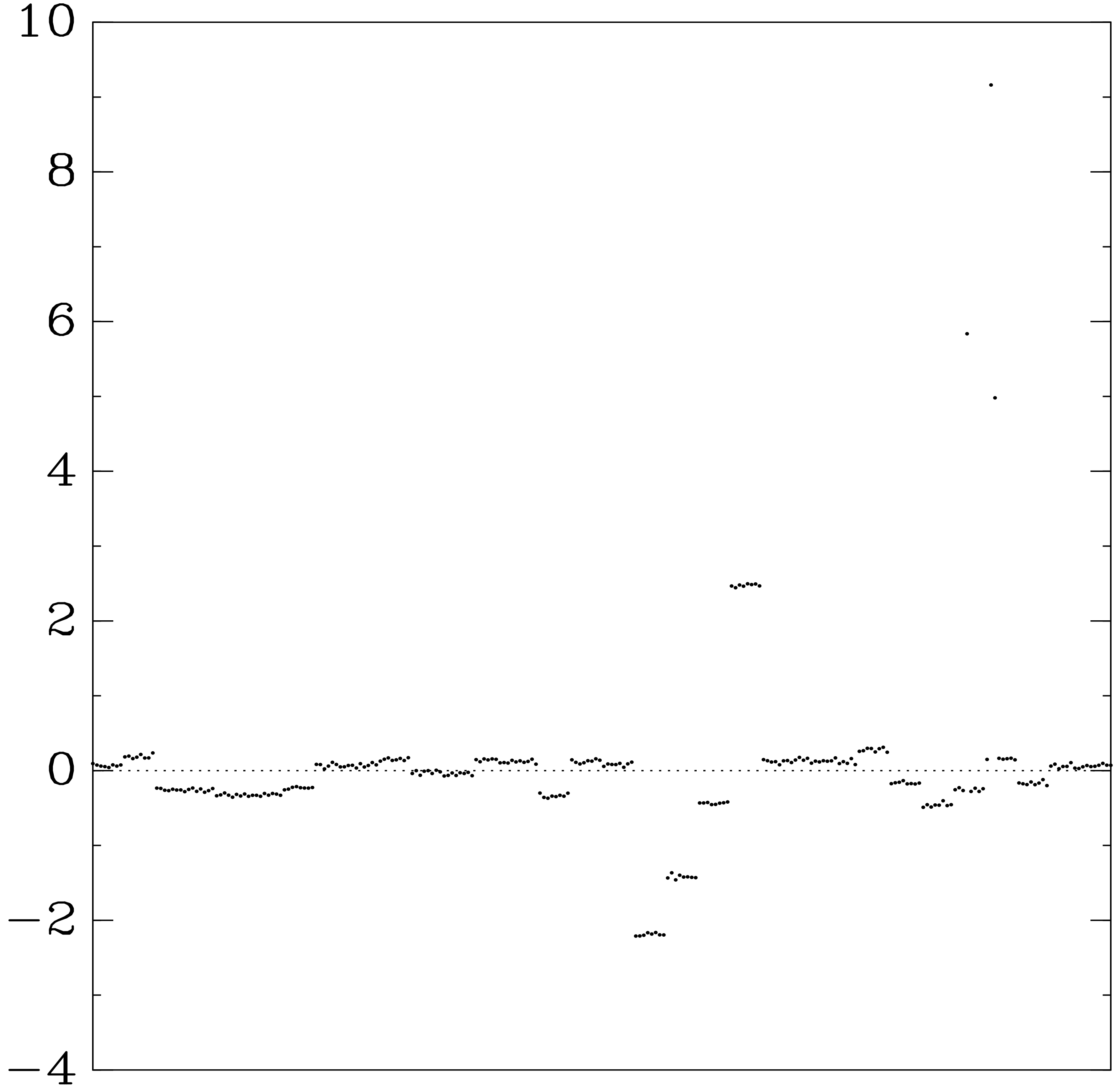
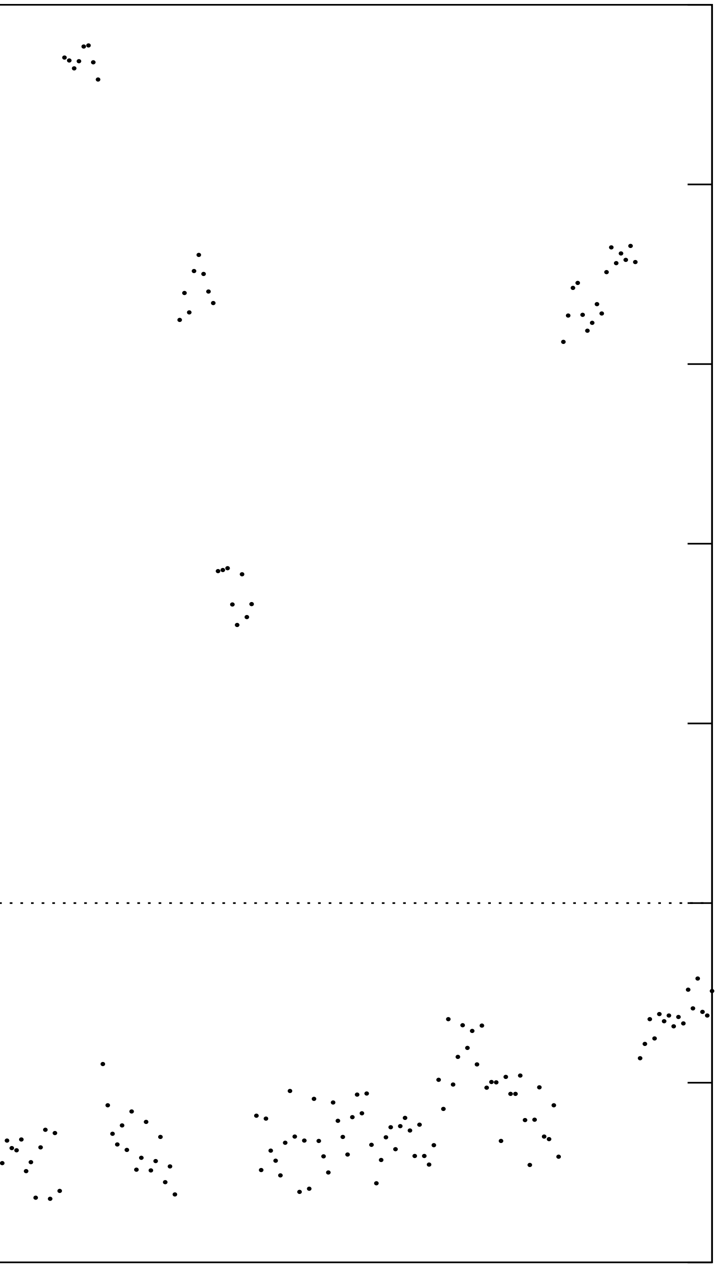


This graph has much larger max, presumably L1 cache miss.



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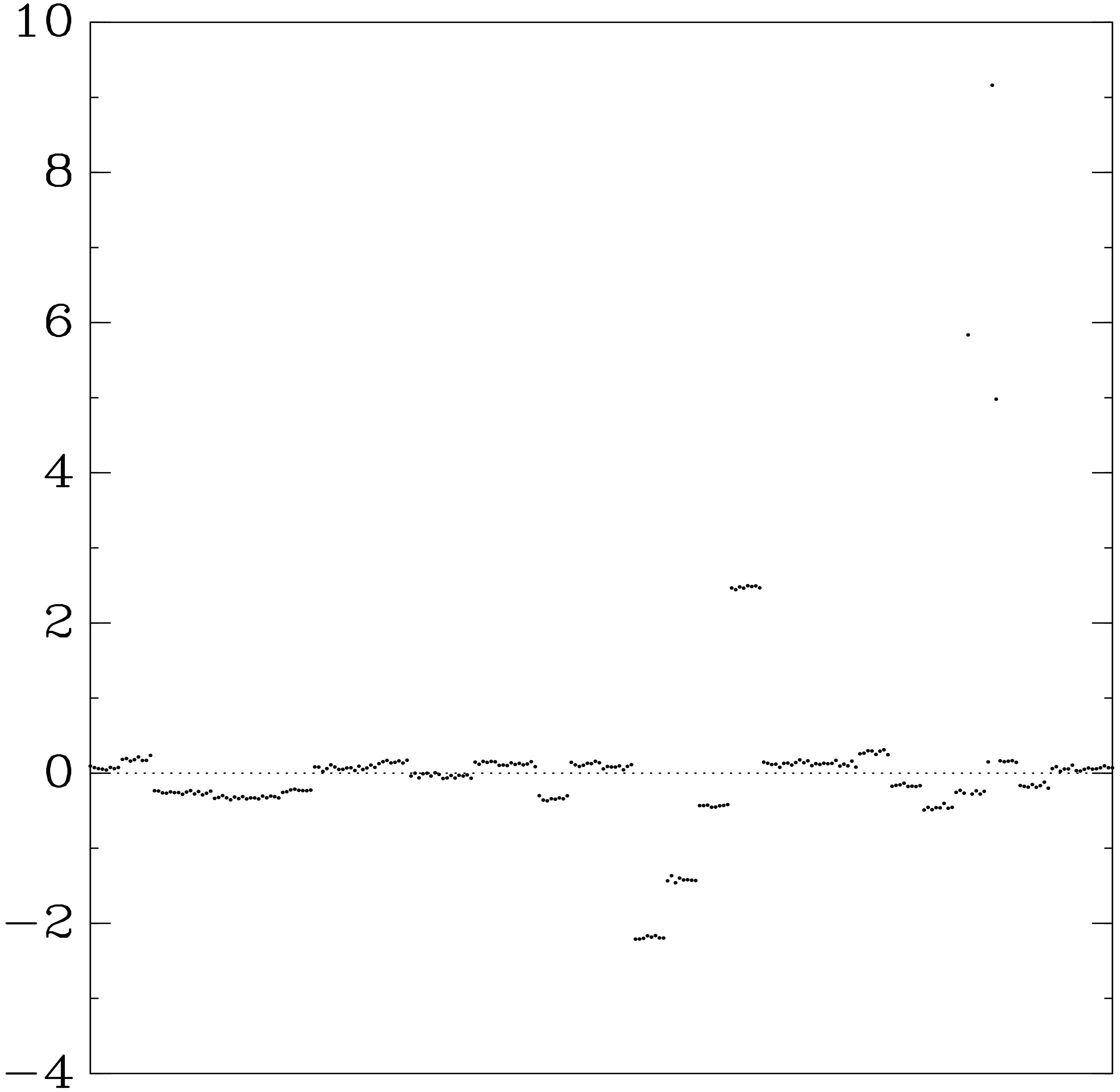

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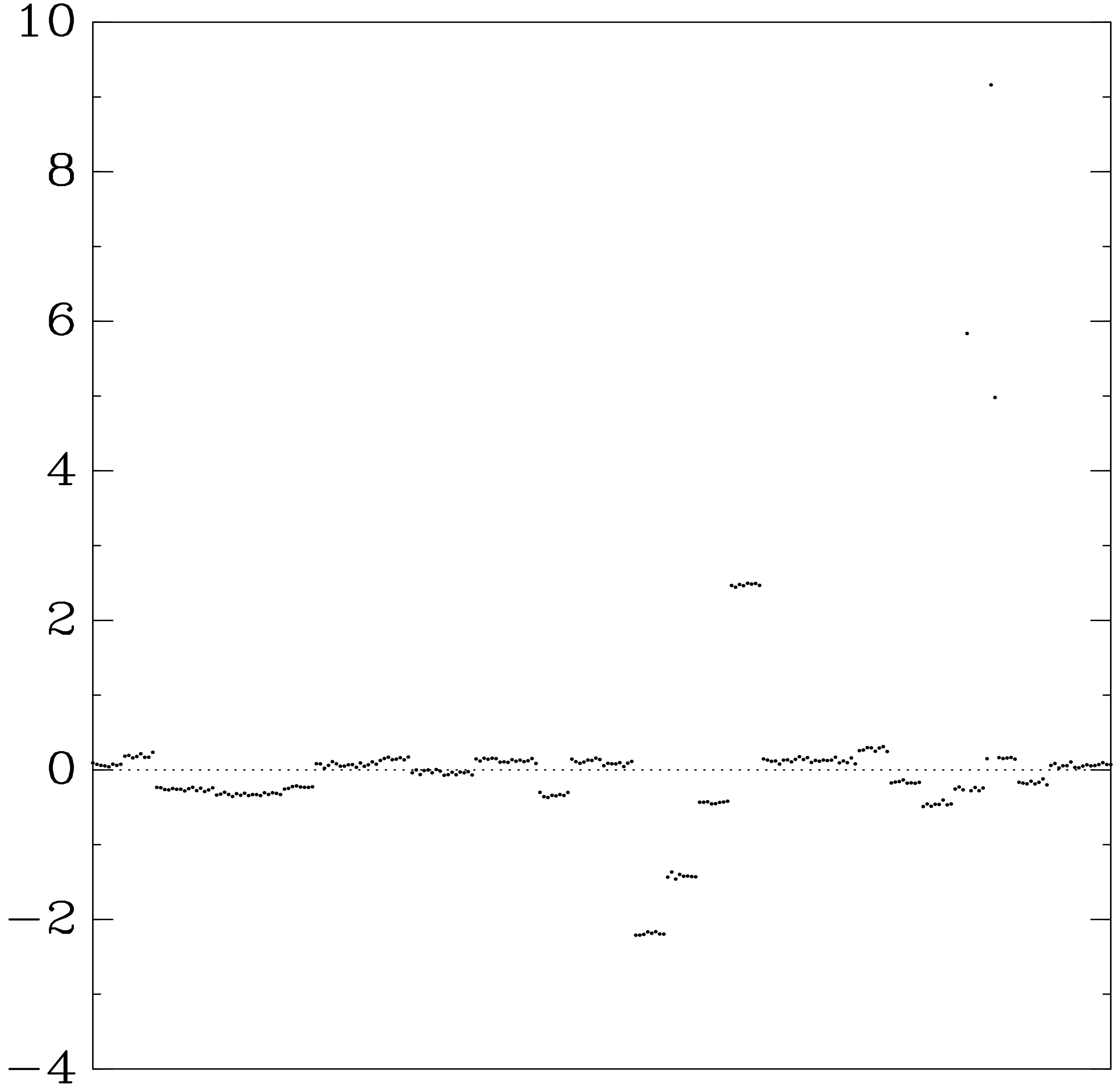

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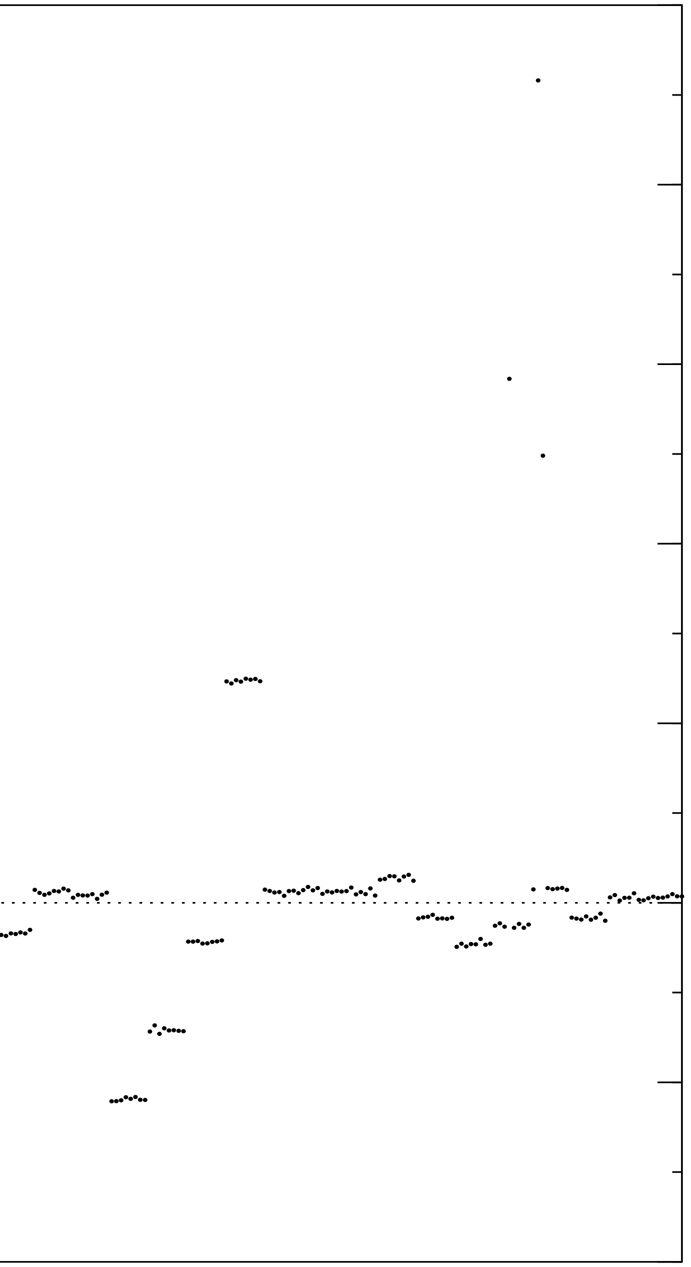

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7. Misdesigning cryptography

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For timing attacks: If attack hasn't been demonstrated, assume it doesn't work.

Don't use obviously-constant-time software such as Phelix.

Don't use cryptographic hardware.

Build complex multi-layer cryptographic systems.
Don't communicate adequately between people designing different layers.

e.g. Most CPU designers fail to thoroughly document CPU speed.

Challenge: Market a CPU with a variable-time adder.